MC33078, MC33079

Low Noise Dual/Quad Operational Amplifiers

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions and is available in the plastic DIP and SOIC packages (P and D suffixes).

- Dual Supply Operation: ±5.0 V to ±18 V
- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/μs
- High Open Loop AC Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/ −14.6 V
- ESD Diodes Provided on the Inputs

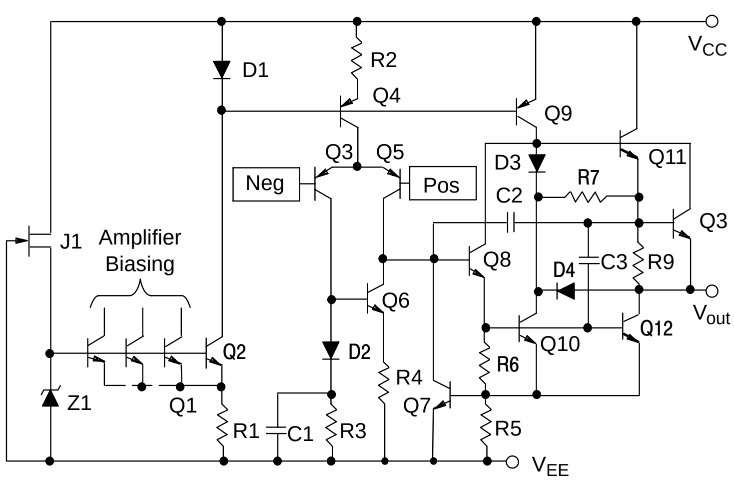


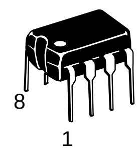
Figure 1. Representative Schematic Diagram
(Each Amplifier)

ON Semiconductor®

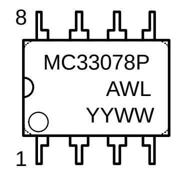
http://onsemi.com

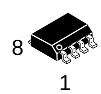
MARKING DIAGRAMS

DUAL

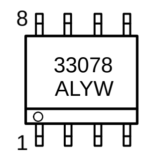


PDIP−8
P SUFFIX
CASE 626

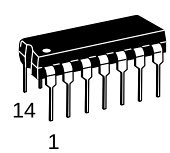




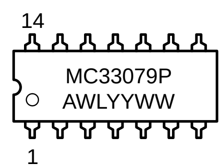
SO−8
D SUFFIX
CASE 751

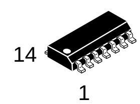


QUAD

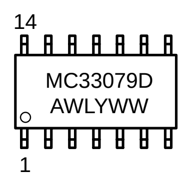


PDIP−14
P SUFFIX
CASE 646





SO−14
D SUFFIX
CASE 751A



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

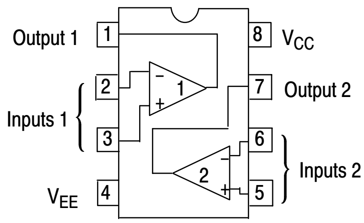
ORDERING INFORMATION

Device	Package	Shipping
MC33078D	SO−8	98 Units/Rail
MC33078DR2	SO−8	2500 Tape & Reel
MC33078P	PDIP−8	50 Units/Rail
MC33079D	SO−14	55 Units/Rail
MC33079DR2	SO−14	2500 Tape & Reel
MC33079P	PDIP−14	25 Units/Rail

PIN CONNECTIONS

DUAL

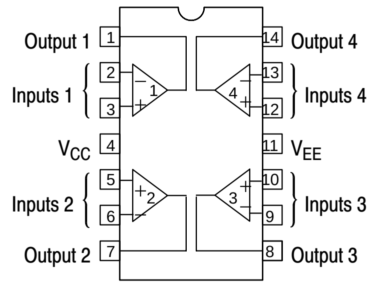
CASE 626/751



(Dual, Top View)

QUAD

CASE 646/751A



(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
ESD Protection at any Pin MC33078 − Human Body Model − Machine Model MC33079 − Human Body Model − Machine Model	V_{esd}	 600 200 550 150	V
Maximum Power Dissipation	P_D	Note 2	mW
Operating Temperature Range	T_A	−40 to +85	°C

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) (MC33078) T_A = +25°C T_A = −40° to +85°C (MC33079) T_A = +25°C T_A = −40° to +85°C	$\|V_{IO}\|$	 – – – –	 0.15 – 0.15 –	 2.0 3.0 2.5 3.5	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	2.0	–	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = −40° to +85°C	I_{IB}	 – –	 300 –	 750 800	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = −40° to +85°C	I_{IO}	 – –	 25 –	 150 175	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13	±14	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = −40° to +85°C	A_{VOL}	 90 85	 110 –	 – –	dB
Output Voltage Swing (V_{ID} = ±1.0V) R_L = 600 Ω R_L = 600 Ω R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_O+ V_O− V_O+ V_O− V_O+ V_O−	 – – +13.2 – +13.5 –	 +10.7 −11.9 +13.8 −13.7 +14.1 −14.6	 – – – −13.2 – −14	V
Common Mode Rejection (V_{in} = ±13V)	CMR	80	100	–	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/ −15 V to +5.0 V/ −5.0 V	PSR	80	105	–	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground) Source Sink	I_{SC}	 +15 −20	 +29 −37	 – –	mA
Power Supply Current (V_O = 0 V, All Amplifiers) (MC33078) T_A = +25°C T_A = −40° to +85°C (MC33079) T_A = +25°C T_A = −40° to +85°C	I_D	 – – – –	 4.1 – 8.4 –	 5.0 5.5 10 11	mA

3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF A_V = +1.0)	SR	5.0	7.0	−	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	10	16	−	MHz
Unity Gain Bandwidth (Open Loop)	BW	−	9.0	−	MHz
Gain Margin (R_L = 2.0 kΩ) C_L = 0 pF C_L = 100 pF	A_m	 − −	 −11 −6.0	 − −	dB
Phase Margin (R_L = 2.0 kΩ) C_L = 0 pF C_L = 100 pF	ϕ_m	 − −	 55 40	 − −	Deg
Channel Separation (f = 20 Hz to 20 kHz)	CS	−	−120	−	dB
Power Bandwidth (V_O = 27 V_{pp}, R_L = 2.0 kΩ, THD ± 1.0%)	BW_p	−	120	−	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	−	0.002	−	%
Open Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)	$\lvert Z_O \rvert$	−	37	−	Ω
Differential Input Resistance ($V_{CM = 0 V}$)	R_{in}	−	175	−	kΩ
Differential Input Capacitance ($V_{CM = 0 V}$)	C_{in}	−	12	−	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	−	4.5	−	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	−	0.5	−	pA/$\sqrt{Hz}$

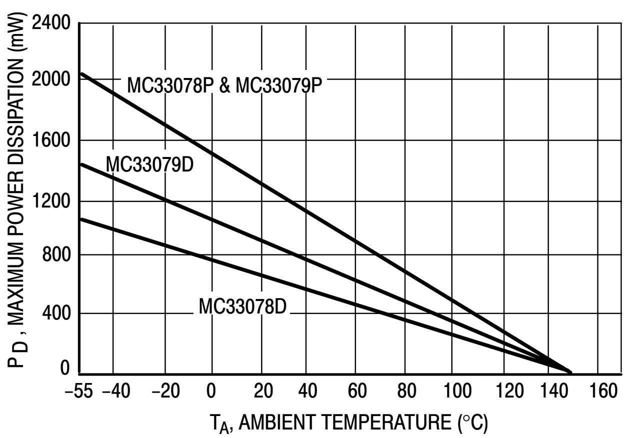


Figure 2. Maximum Power Dissipation versus Temperature

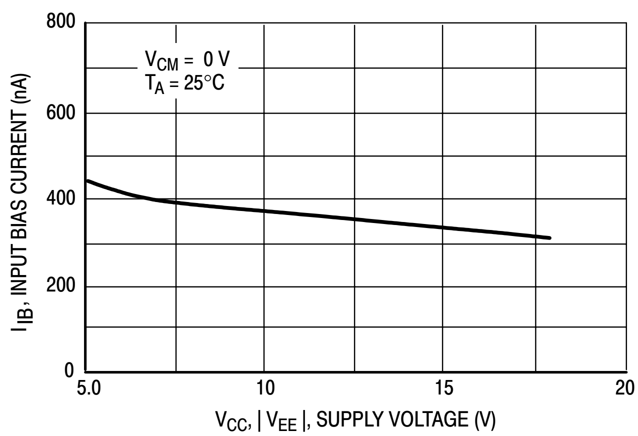


Figure 3. Input Bias Current versus Supply Voltage

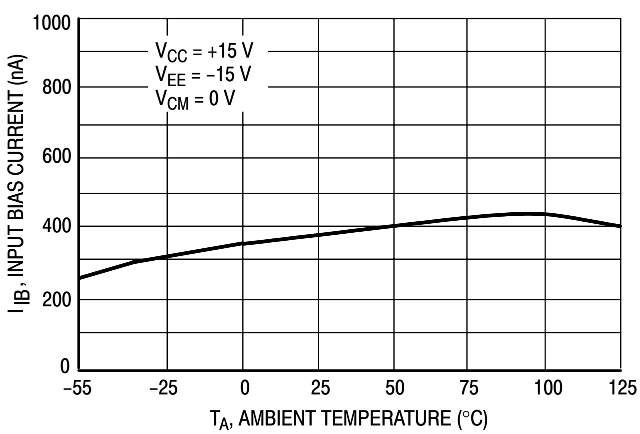


Figure 4. Input Bias Current versus Temperature

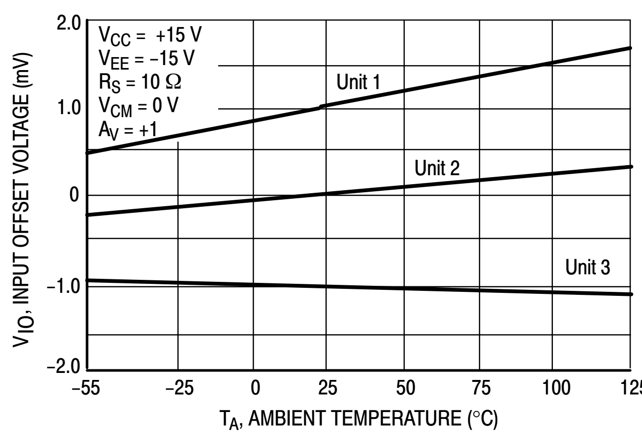


Figure 5. Input Offset Voltage versus Temperature

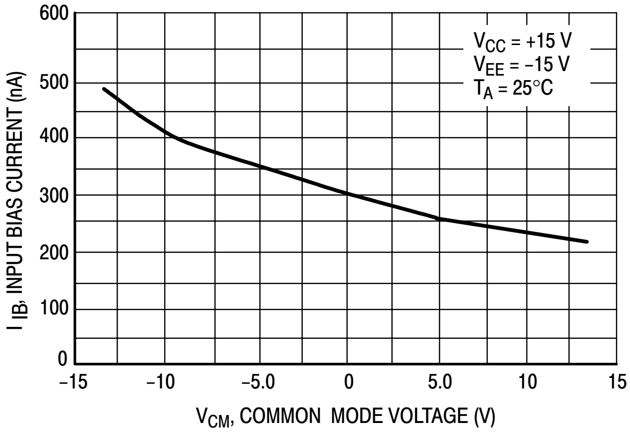


Figure 6. Input Bias Current versus Common Mode Voltage

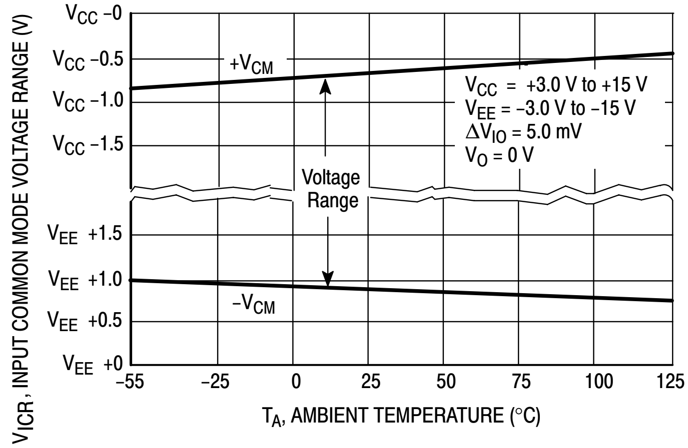


Figure 7. Input Common Mode Voltage Range versus Temperature

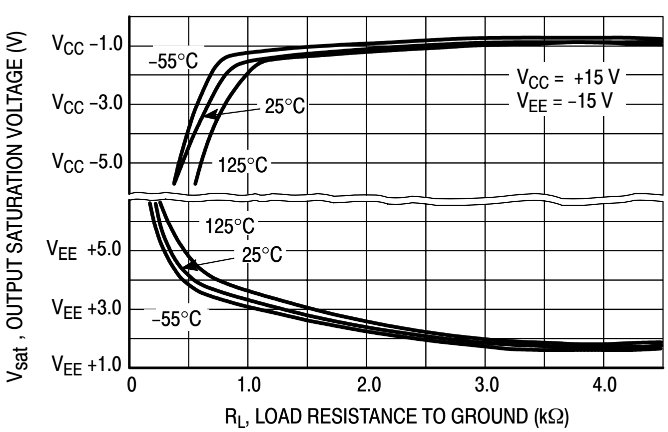


Figure 8. Output Saturation Voltage versus Load Resistance to Ground

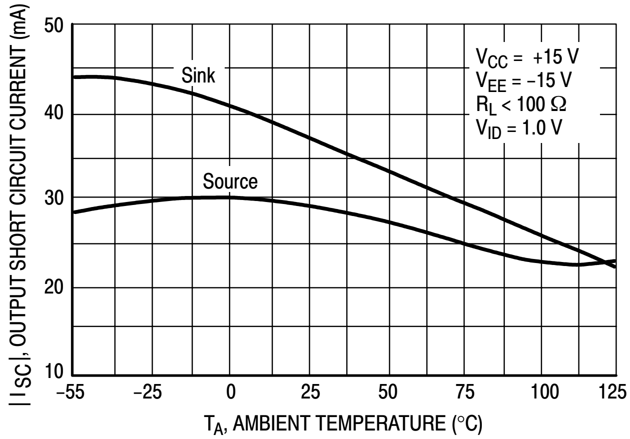


Figure 9. Output Short Circuit Current versus Temperature

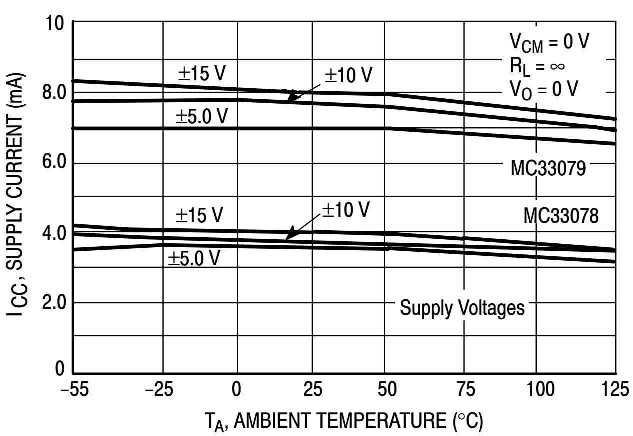


Figure 10. Supply Current versus Temperature

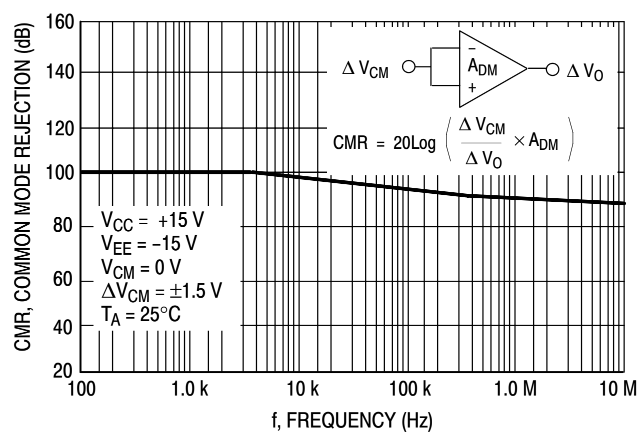


Figure 11. Common Mode Rejection versus Frequency

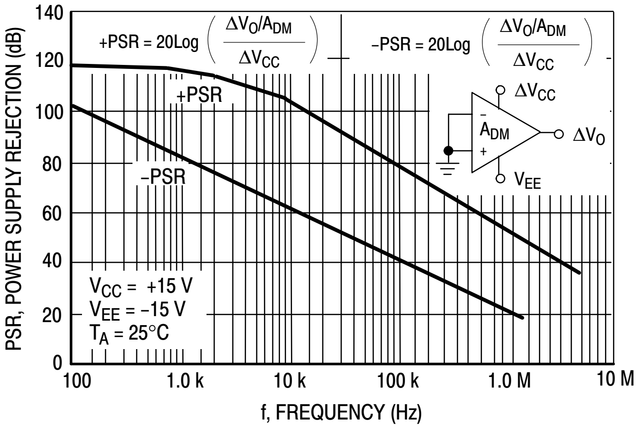


Figure 12. Power Supply Rejection versus Frequency

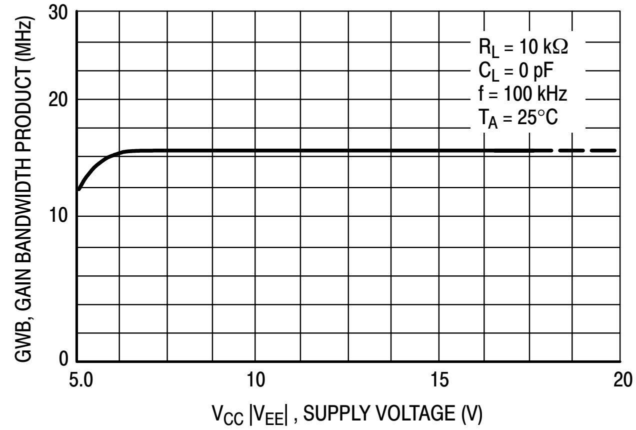


Figure 13. Gain Bandwidth Product versus Supply Voltage

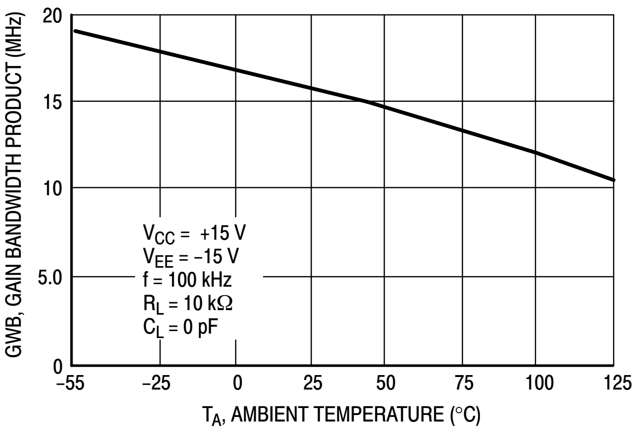


Figure 14. Gain Bandwidth Product versus Temperature

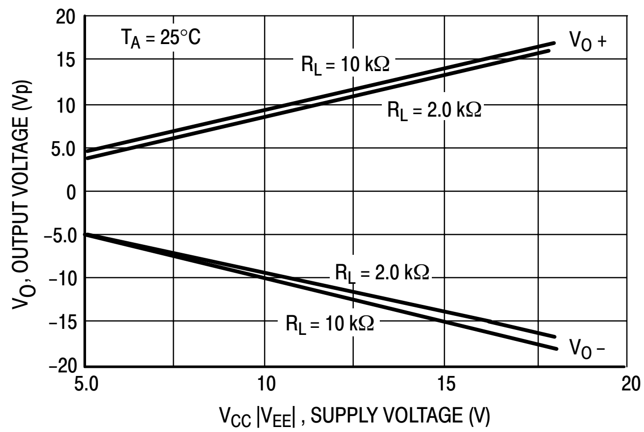


Figure 15. Maximum Output Voltage versus Supply Voltage

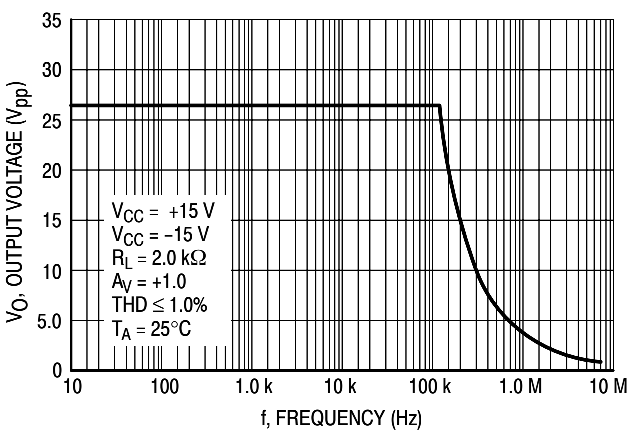


Figure 16. Output Voltage versus Frequency

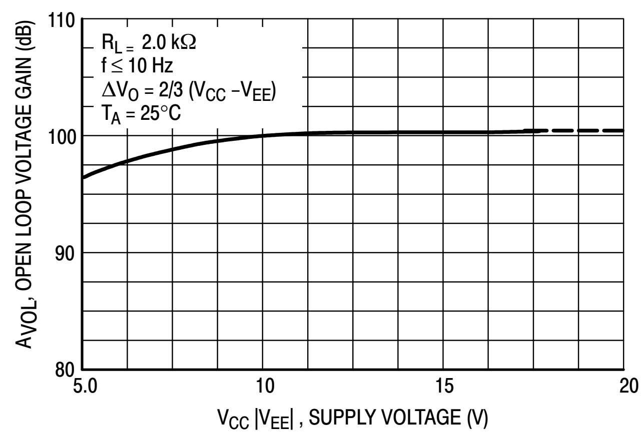


Figure 17. Open Loop Voltage Gain versus Supply Voltage

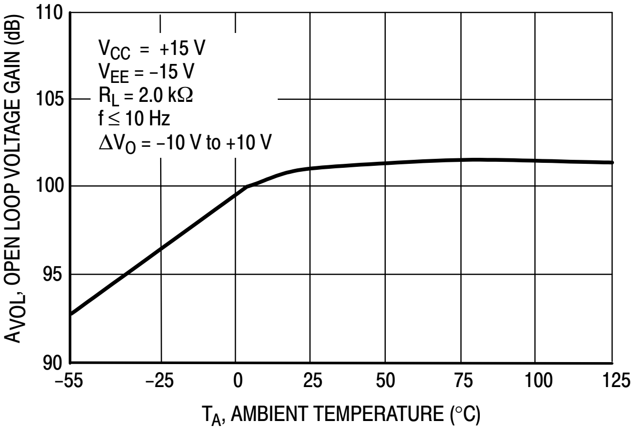


Figure 18. Open Loop Voltage Gain versus Temperature

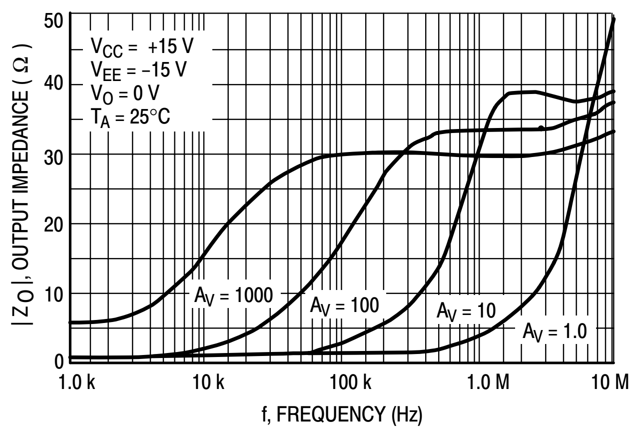


Figure 19. Output Impedance versus Frequency

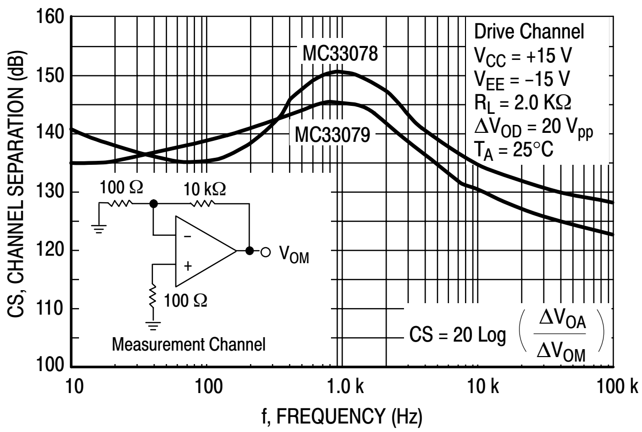


Figure 20. Channel Separation versus Frequency

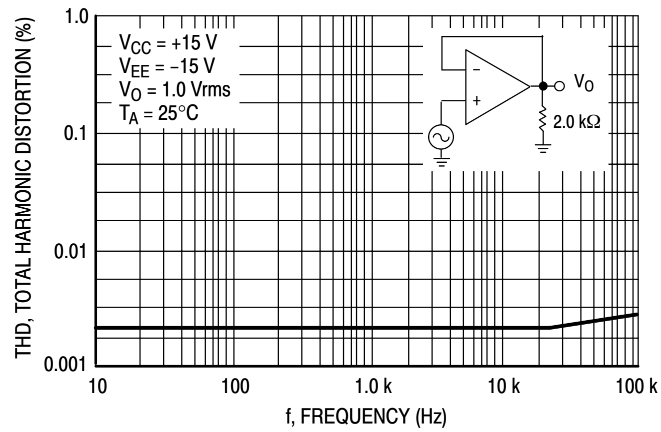


Figure 21. Total Harmonic Distortion versus Frequency

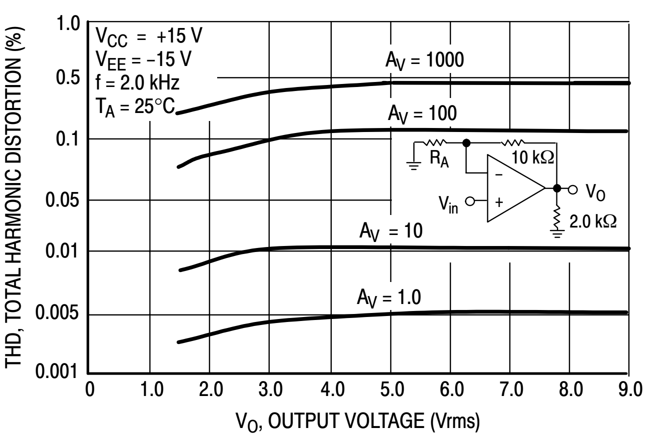


Figure 22. Total Harmonic Distortion versus Output Voltage

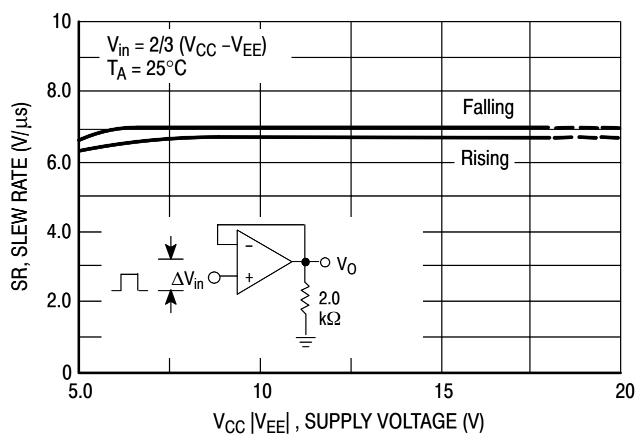


Figure 23. Slew Rate versus Supply Voltage

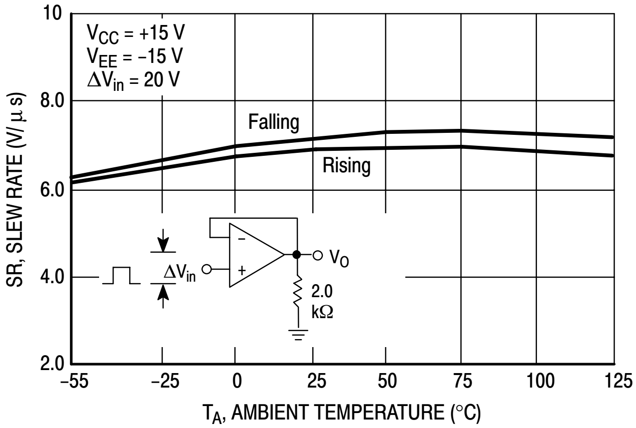


Figure 24. Slew Rate versus Temperature

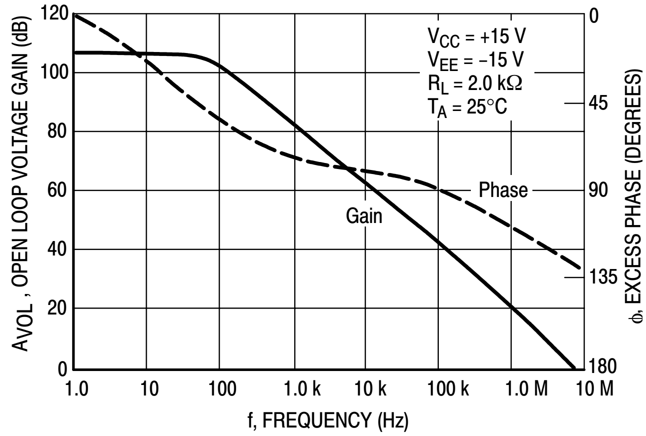


Figure 25. Voltage Gain and Phase versus Frequency

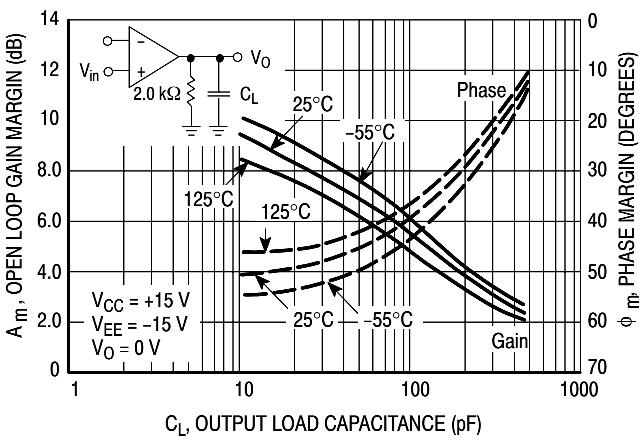


Figure 26. Open Loop Gain Margin and Phase Margin versus Load Capacitance

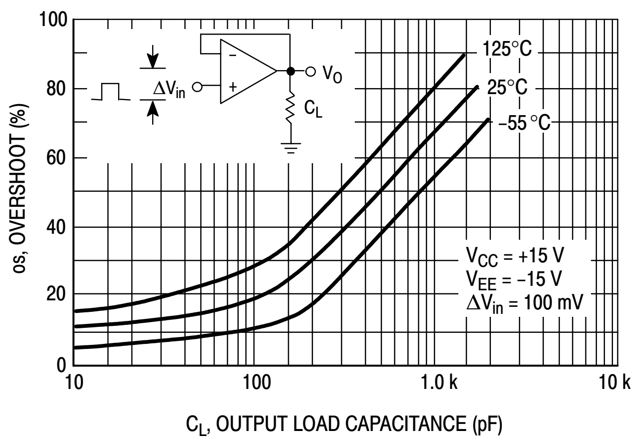


Figure 27. Overshoot versus Output Load Capacitance

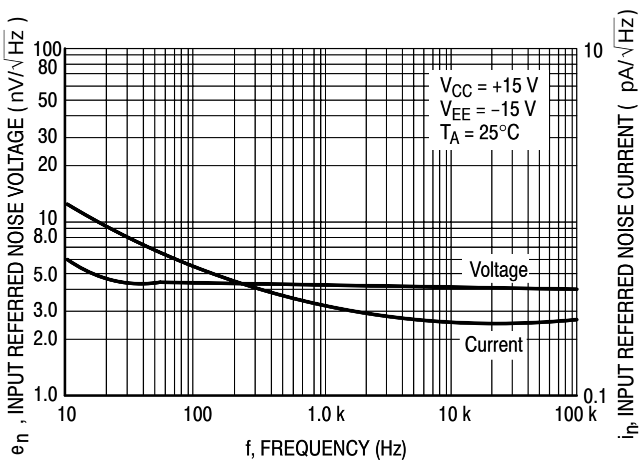


Figure 28. Input Referred Noise Voltage and Current versus Frequency

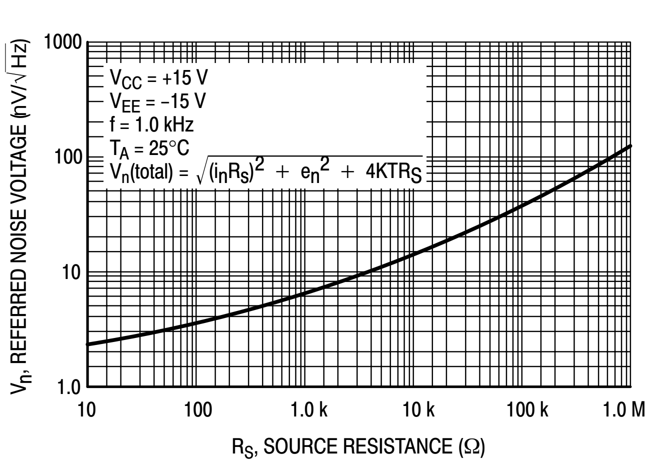


Figure 29. Total Input Referred Noise Voltage versus Source Resistance

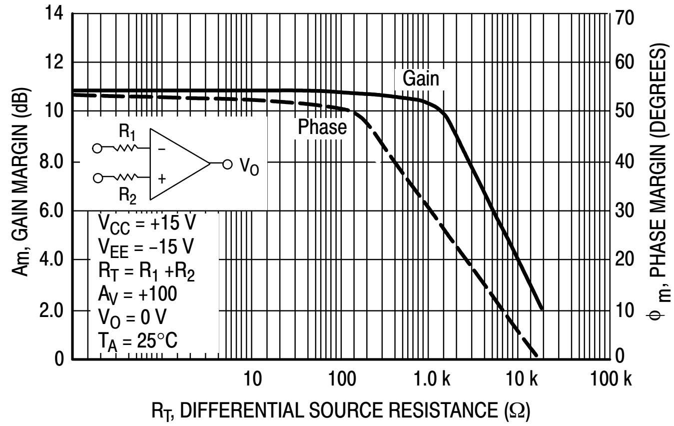


Figure 30. Phase Margin and Gain Margin versus Differential Source Resistance

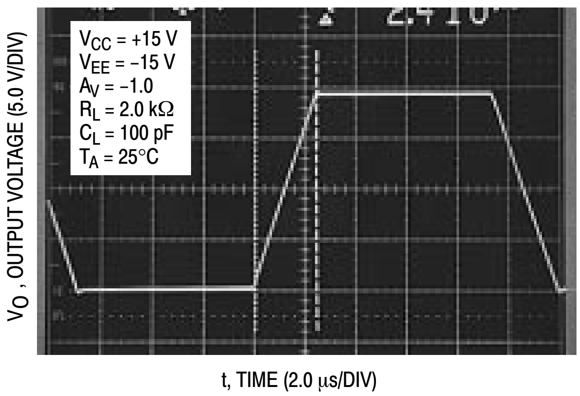


Figure 31. Inverting Amplifier Slew Rate

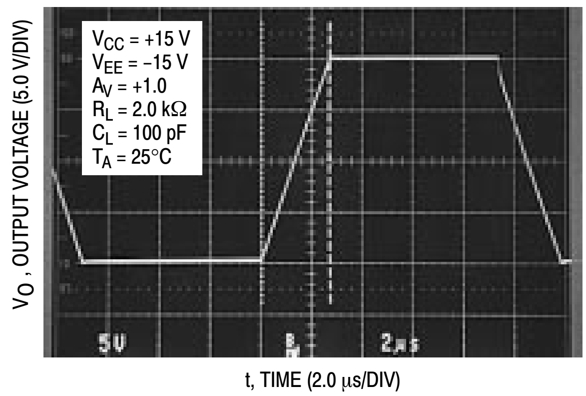


Figure 32. Non−inverting Amplifier Slew Rate

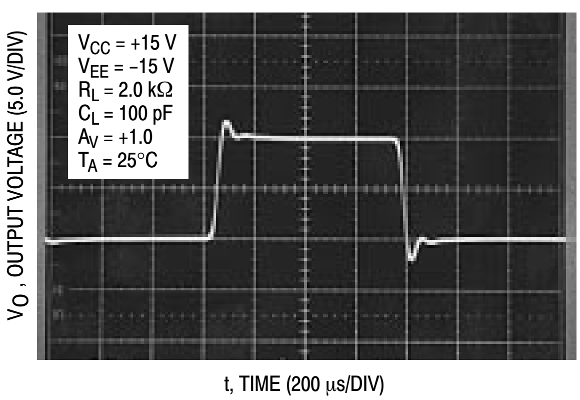


Figure 33. Non−inverting Amplifier Overshoot

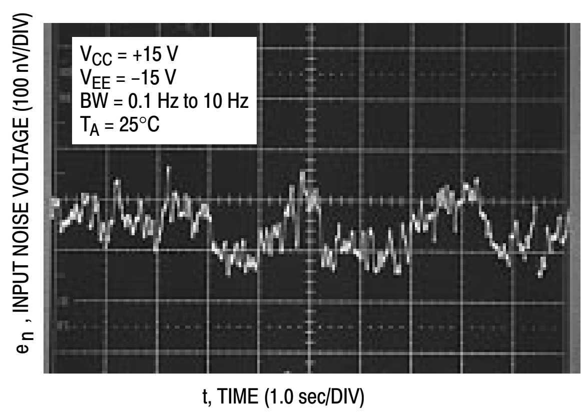
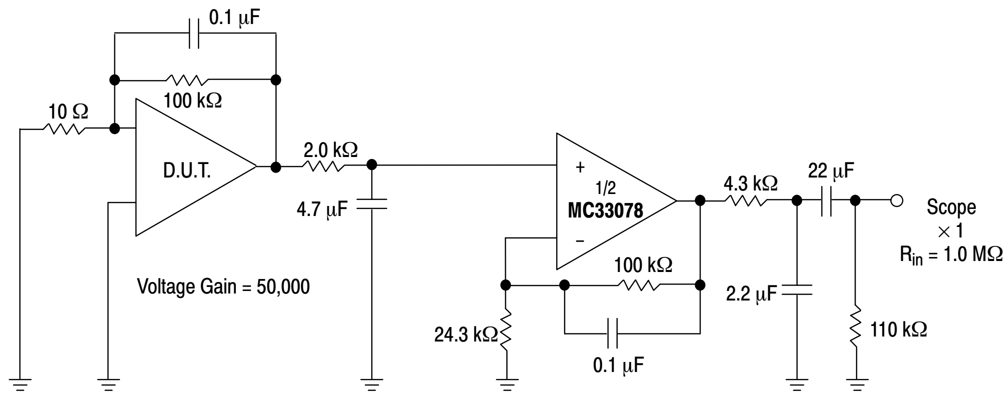


Figure 34. Low Frequency Noise Voltage versus Time

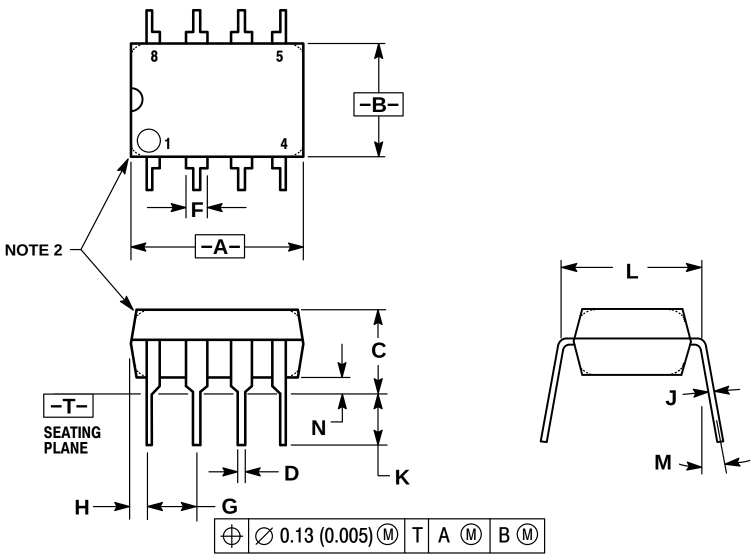


Note: All capacitors are non−polarized.

Figure 35. Voltage Noise Test Circuit
(0.1 Hz to 10 Hz_{p-p})

PACKAGE DIMENSIONS

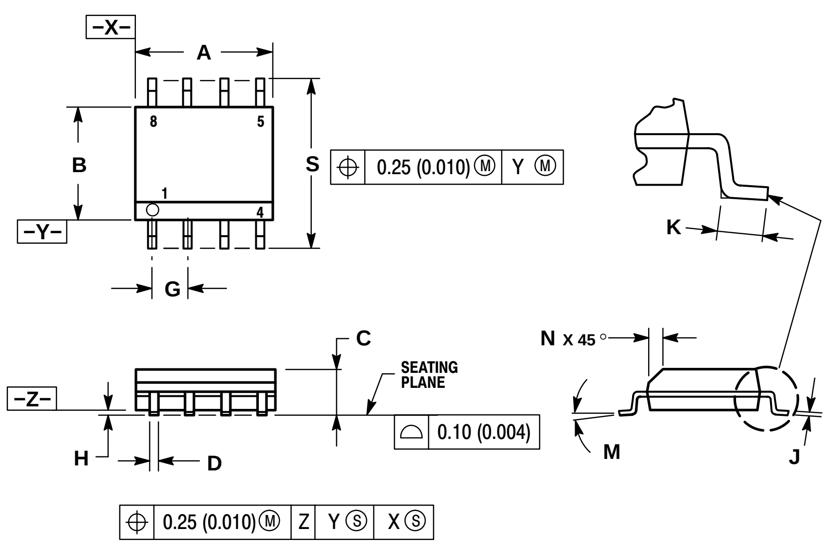
PDIP−8
P SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO−8
D SUFFIX
CASE 751−07
ISSUE AA

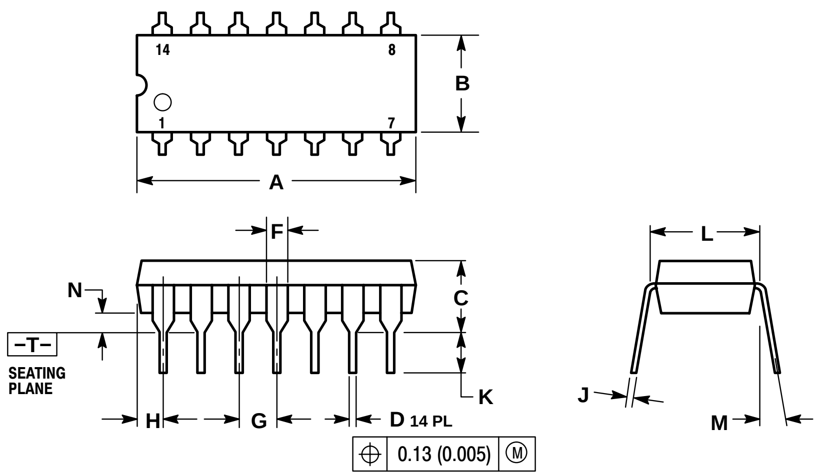


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

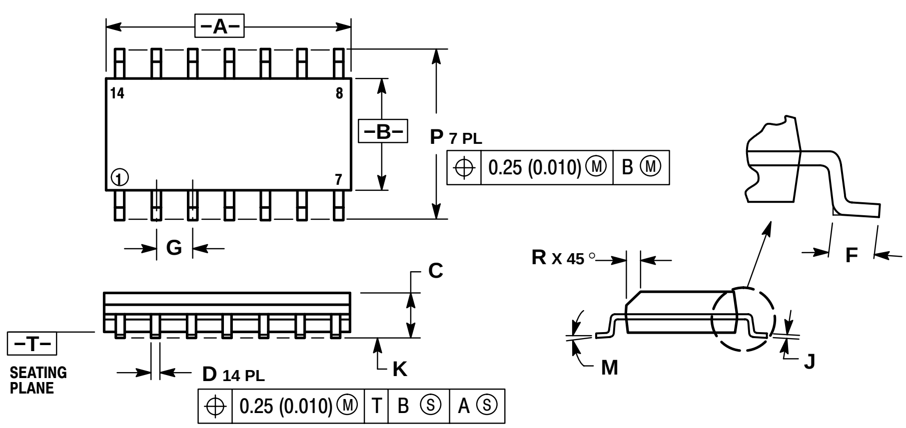
PDIP−14
P SUFFIX
CASE 646−06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SO−14
D SUFFIX
CASE 751A−03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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