DATA SHEET

74LVC244A
74LVCH244A

Octal buffer/line driver with 5 Volt tolerant input/outputs; 3-state

Product specification
File under Integrated Circuits, IC24

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Philips
Semiconductors

PHILIPS

Octal buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC244A 74LVCH244A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range of 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- High impedance when VCC = 0 V
- Bushold on all data inputs (74LVCH244A only)
- Specified from –40 to +85 and +125 °C.

DESCRIPTION

The 74LVC244A/74LVCH244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC244A/74LVCH244A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The ‘244’ is functionally identical to the ‘240’, but the ‘240’ has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	C_L = 50 pF; V_{CC} = 3.3 V	2.8	ns
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V; notes 1 and 2	10	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in V;

   N = total switching outputs;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC244AD	–40 to +125 °C	20	SO	plastic	SOT163-1
74LVC244ADB		20	SSOP	plastic	SOT339-1
74LVC244APW		20	TSSOP	plastic	SOT402-1
74LVC244ABQ		20	DQFN20	plastic	SOT764-1
74LVCH244AD		20	SO	plastic	SOT163-1
74LVCH244ADB		20	SSOP	plastic	SOT339-1
74LVCH244APW		20	TSSOP	plastic	SOT402-1
74LVCH244ABQ		20	DQFN20	plastic	SOT764-1

FUNCTION TABLE

See note 1.

INPUTS		OUTPUTS
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high impedance OFF-state.

PINNING

SYMBOL	DESCRIPTION
$1\overline{OE}$	output enable input (active LOW)
$1A_0$ to $1A_3$	data inputs
$2Y_0$ to $2Y_3$	bus outputs
GND	ground (0 V)
$2A_3$ to $2A_0$	data inputs
$1Y_3$ to $1Y_0$	bus outputs
$2\overline{OE}$	output enable input (active LOW)
V_{CC}	DC supply voltage

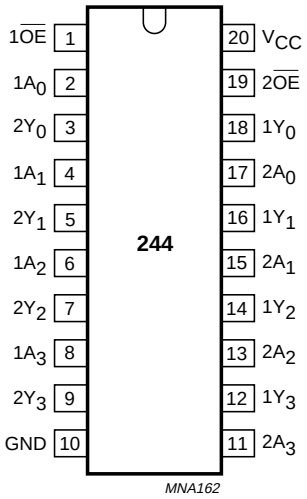
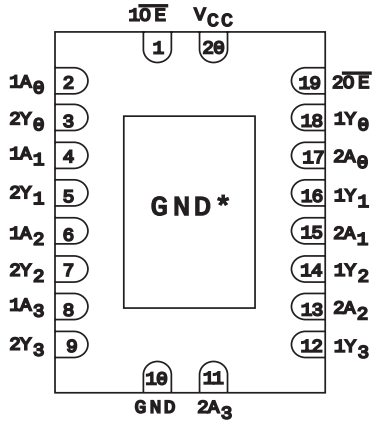


Fig.1 Pin configuration for SO SSOP and TSSOP.



* The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration for DQFN20 (Top view).

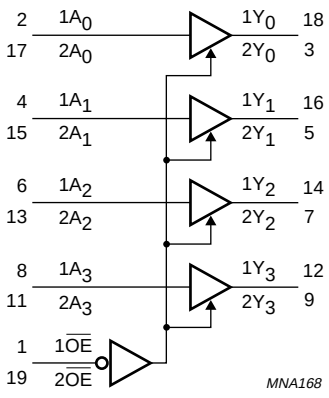


Fig.3 Logic symbol.

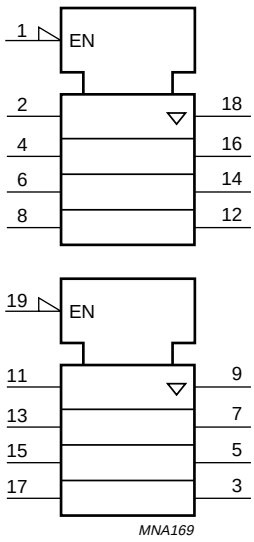


Fig.4 Logic symbol (IEEE/IEC).

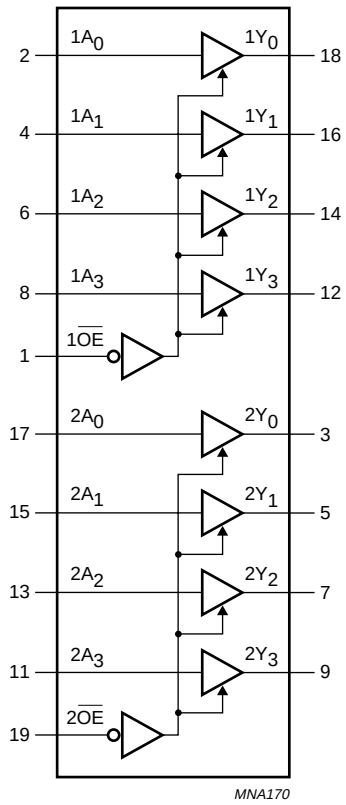


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		CONDITIONS	LIMITS		UNIT
				MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)			2.7	3.6	V
	DC supply voltage (for low-voltage applications)			1.2	3.6	V
V_I	DC input voltage range			0	5.5	V
V_O	DC output voltage range	output HIGH or LOW state		0	V_{CC}	V
		output 3-state		0	5.5	V
T_{amb}	operating ambient temperature range			–40	+125	°C
t_r,t_f	input rise and fall times		V_{CC} = 1.2 to 2.7 V	0	20	ns/V
			V_{CC} = 2.7 to 3.6 V	0	10	

LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 60134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER		CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage			–0.5	+6.5	V
I_{IK}	DC input diode current		V_I < 0	–	–50	mA
V_I	DC input voltage		note 1	–0.5	+6.5	V
I_{OK}	DC output diode current		V_O > V_{CC} or V_O < 0	–	±50	mA
V_O	DC output voltage	output HIGH or LOW state	note 1	–0.5	V_{CC} + 0.5	V
		output 3-state	note 1	–0.5	+ 6.5	V
I_O	DC output source or sink current		V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current			–	±100	mA
T_{stg}	storage temperature range			–65	+150	°C
P_{tot}	power dissipation per package		for temperature range: –40 to +125 °C; note 2	–	500	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO packages: above 70 °C the value of P_D derates linearly with 8 mW/K.
   For TSSOP packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.
   For DQFN20 packages: above 60 °C the value of P_D derates linearly with 4.5 mW/K.

DC CHARACTERISTICS

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			T_{amb} (°C)		UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V_{CC}	–	V
			2.7 to 3.6	2.0	–	–	2.0	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	–	GND	V
			2.7 to 3.6	–	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage; V_I = V_{IH} or V_{IL}	I_O = –100 µA	2.7 to 3.6	V_{CC} – 0.2	V_{CC}	–	V_{CC} – 0.3	–	V
		I_O = –12 mA	2.7	V_{CC} – 0.5	–	–	V_{CC} – 0.65	–	V
		I_O = –18 mA	3.0	V_{CC} – 0.6	–	–	V_{CC} – 0.75	–	V
		I_O = –24 mA	3.0	V_{CC} – 0.8	–	–	V_{CC} – 1	–	V
V_{OL}	LOW-level output voltage; V_I = V_{IH} or V_{IL}	I_O = 100 µA	2.7 to 3.6	–	GND	0.2	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.4	–	0.6	V
		I_O = 24 mA	3.0	–	–	0.55	–	0.8	V
I_I	input leakage current	V_I = 5.5 V or GND; note 6	3.6	–	±0.1	±5	–	±20	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL};(6) V_O = 5.5 V or GND	3.6	–	0.1	±5	–	±20	µA
I_{off}	power off leakage supply	V_I or V_O = 5.5 V	0.0	–	0.1	±10	–	±20	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.1	10	–	40	µA
ΔI_{CC}	additional quiescent supply current per in. pin	V_I =V_{CC}–0.6V; I_O = 0	2.7 to 3.6	–	5	500	–	5000	µA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V: notes 2, 3 and 4	3.0	75	–	–	60	–	µA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V: notes 2, 3 and 4	3.0	–75	–	–	–60	–	µA
I_{BHLO}	bushold LOW overdrive current	notes 2, 3 and 5	3.6	500	–	–	500	–	µA
I_{BHHO}	bushold HIGH overdrive current	notes 2, 3 and 5	3.6	–500	–	–	–500	–	µA

Notes

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when V_I exceeds V_{CC} allowing 5.5 V on the input terminal.

AC CHARACTERISTICS

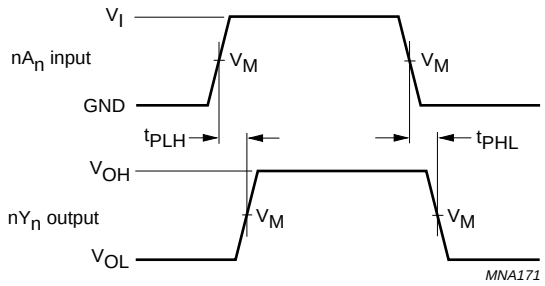
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	WAVEFORMS	T_{amb} (°C)					UNIT
			–40 to +85			–40 to +125		
			MIN.	TYP.	MAX.	MIN.	MAX.	
V_{CC} = 1.2 V; note 1								
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	see Figs 6 and 8	–	17	–	–	–	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	–	24	–	–	–	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	–	9.0	–	–	–	ns
V_{CC} = 2.7 V; note 1								
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	see Figs 6 and 8	1.5	3.3	6.9	1.5	9.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	1.5	4.3	8.6	1.5	11.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	1.5	3.2	6.8	1.5	8.5	ns
V_{CC} = 3.0 to 3.6 V; note 1								
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	see Figs 6 and 8	1.5	2.8	5.9	1.5	7.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	1.0	3.4	7.6	1.0	9.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	1.5	2.9	5.8	1.5	7.5	ns
$t_{sk(0)}$	skew	note 2			1.0		1.5	ns

Notes

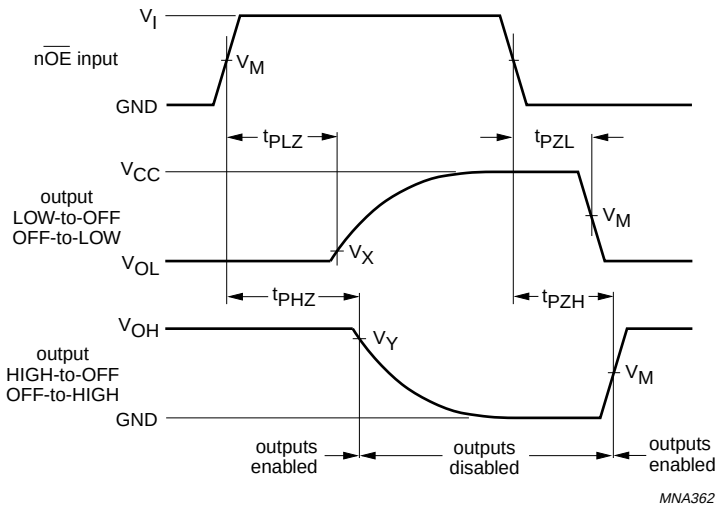
1. Typical values at V_{CC} = 3.3 V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



V_M(1) = 1.5 V at $V_{CC} \geq 2.7$ V;
V_M(1) = 0.5 V_{CC} at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

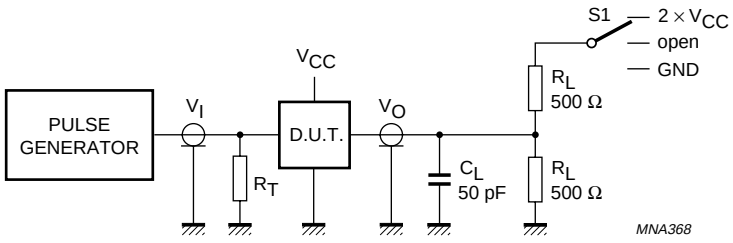
Fig.6 The input nA to output nY propagation delays.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 V_{CC} at V_{CC} < 2.7 V;
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_X = V_{OL}$ + 0.1 V at V_{CC} < 2.7 V;
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_Y = V_{OH}$ − 0.1 V at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.



SWITCH POSITION	
TEST	**SWITCH**
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

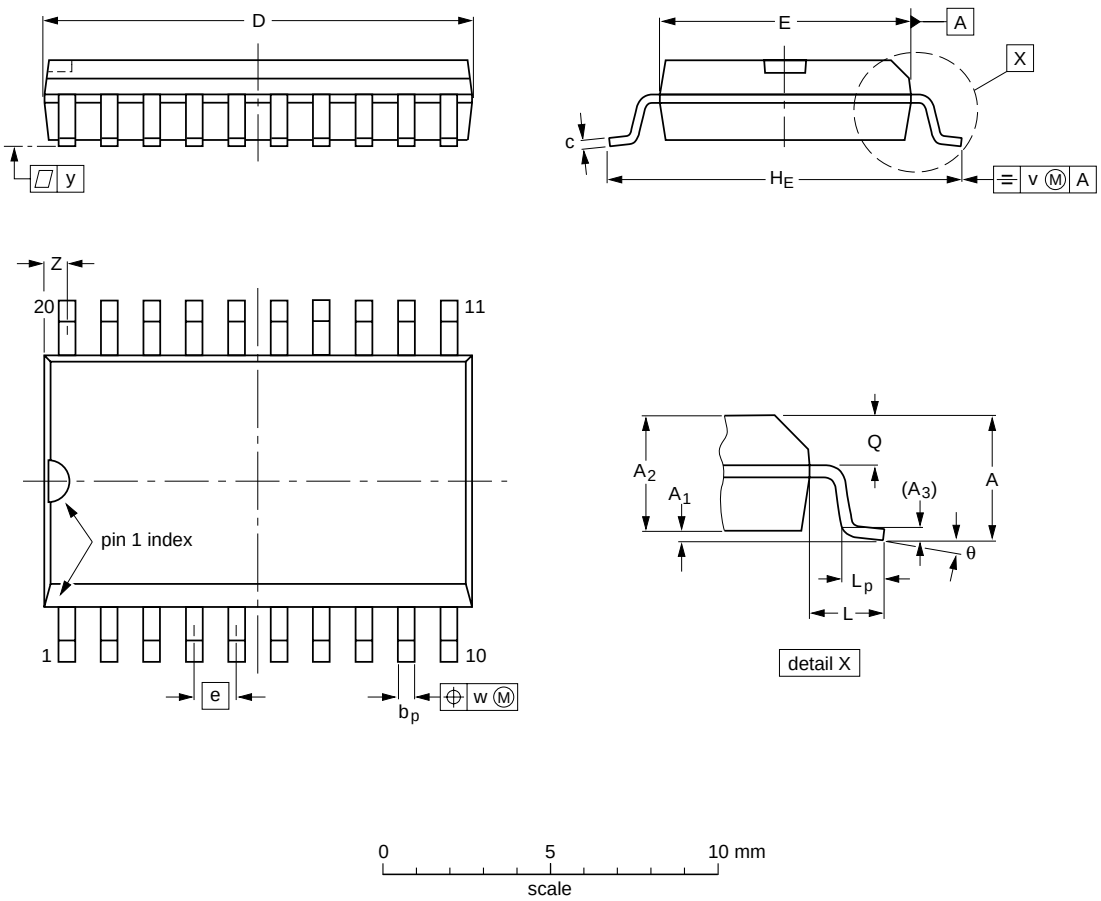
V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Definitions for test circuits:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance (see Chapter “AC characteristics”).
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

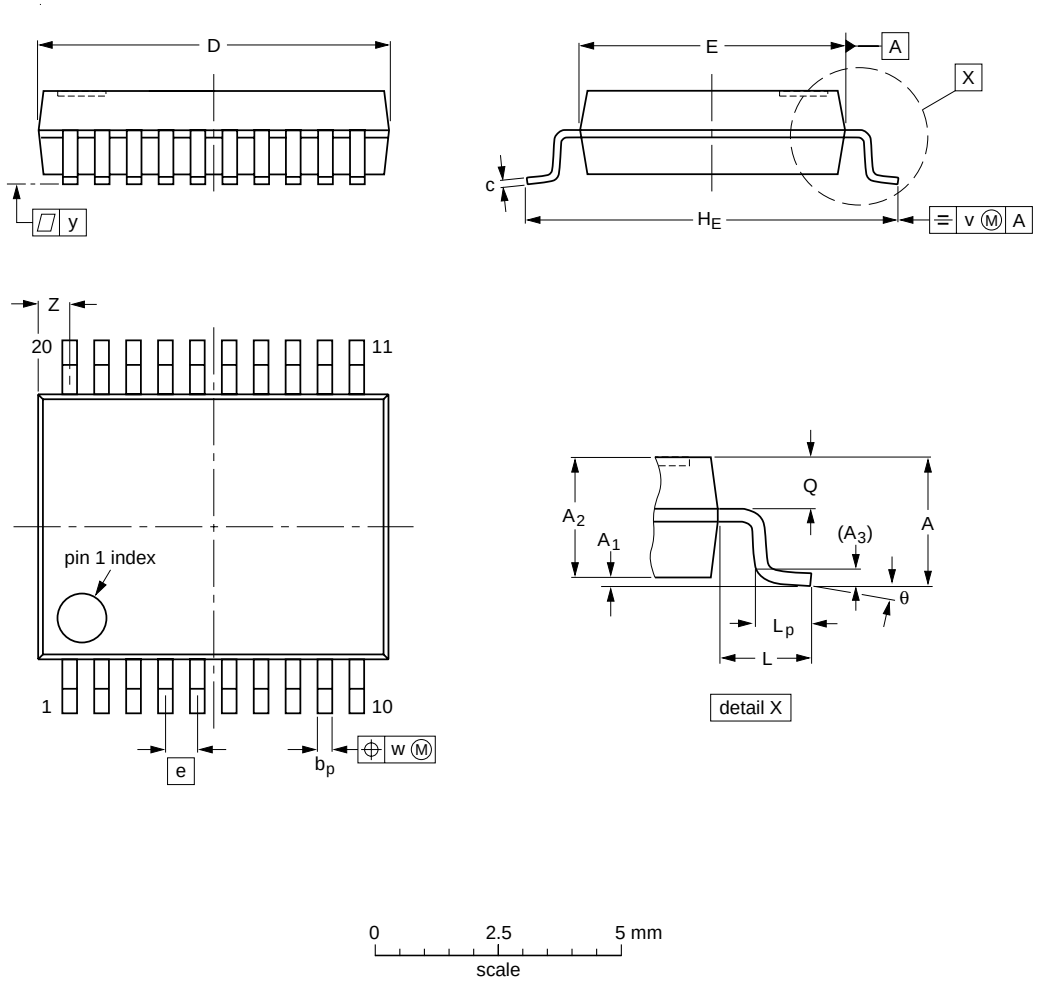
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

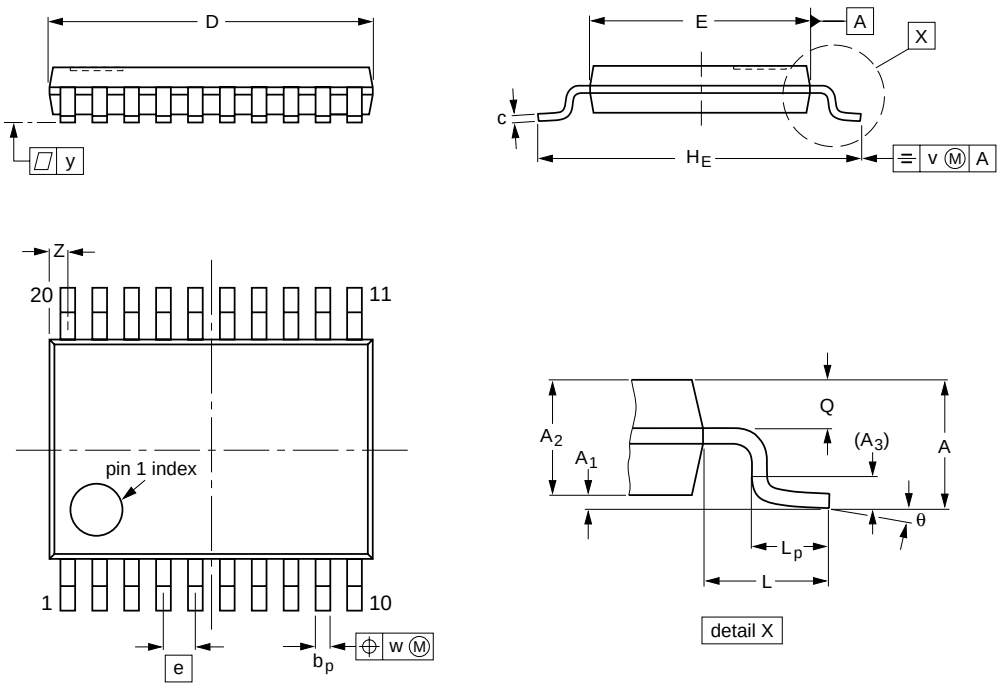
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

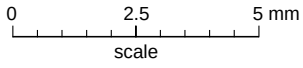
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

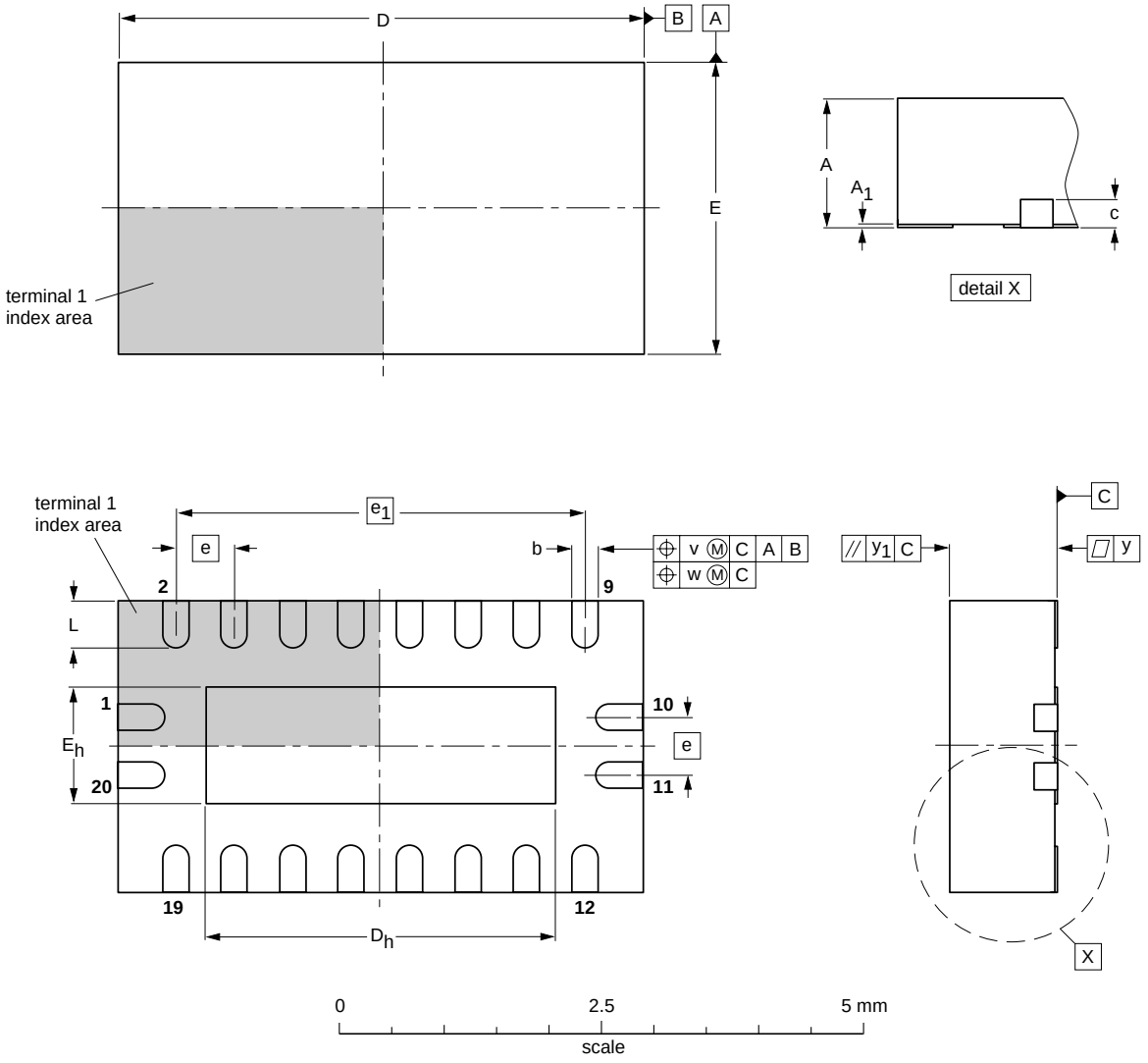
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	- - -	- - -			~~02-07-05~~ 02-10-17

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS, DQFN	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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