

# Follow PC-Board Design Guidelines for Lowest CMOS EMI Radiation

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The application of such high-speed CMOS-logic circuits as the 54HC/74HC family (as compared with CD4000 metal-gate logic) requires special attention to pc-board design to minimize conducted and radiated noise.

The need to reduce a logic system's noise emission is becoming ever more apparent with the increased use of high-speed electronics, and with the progressive tightening of regulations covering the amount of permissible radiated system noise. This article presents empirical and analytical techniques for effective EMI control of 54HC/74HC high-speed CMOS-logic circuitry.

Several sources conduct or radiate EMI from electronic apparatus. Among these are

- antenna loops formed by ICs and their decoupling capacitors
- pc-board traces carrying driving-and driven-chip currents
- common-impedance coupling and crosstalk.

To minimize EMI-related problems, you must reduce all extraneous system noise, reduce the effects of parasitic pc-board trace antennas, and employ effective system shielding. The following sections examine these EMI sources and present techniques of minimizing them for high-speed CMOS logic.

## BEWARE COMMON IMPEDANCES

The most obvious precaution to take in any analog or digital design is to minimize the extent of common-impedance paths. Figure 1 gives a generalized representation of a logic layout in which the earth ground and the signal ground are not common. Methods of reducing EMI focus on the minimization of common-impedance paths, shown here primarily as ground-line impedances  $Z_1$  through  $Z_4$ . Signal-line impedances, though not shown here, could also come into play.

These common impedances result in noise emission, arising from the ground-line voltage drops that occur during current switching; you can generally reduce the drops by enlarging the ground conductor in order to reduce its effective impedance. This action has a secondary advantage: The ground trace can form a shield that reduces emission by other circuit traces, particularly in multilayer circuit boards.

Stray coupling capacitances (shown in Figure 1 as  $C_1$  and  $C_2$ ) that effectively "bridge" signals from one trace to another constitute a second source of noise. These paths can occur as the result of coupling from one pc-board trace to another or, alternatively, from an IC package to the pc board.

Impedances  $Z_1$  through  $Z_4$  are functions of the thickness of the copper pc-board foil, circuit switching speeds and the effective lengths of the traces. The common-impedance paths provide the coupling by which noise currents are injected, circulated and finally returned to any package on the pc board.

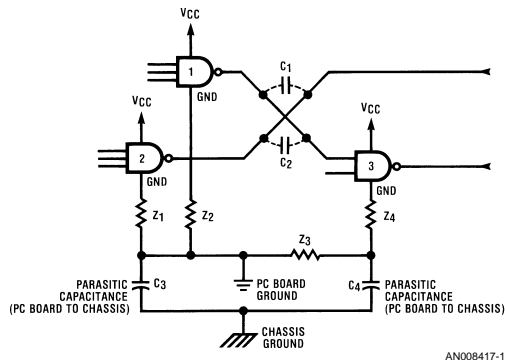
The amount of voltage generated by the noise/switching currents multiplied by the impedances is difficult to predict. However, the higher the impedances, the higher the radiated

noise. An easy empirical method that can serve as a general rule is to render the pc board as optically opaque as possible by making ground and supply trace areas as large as possible (Figure 3). This measure lowers the trace impedances. As a side benefit, it helps to conserve the etchant bath in the manufacturing process.

## MEASURE PC-BOARD NOISE FOR EMI CONTROL

A simple but effective technique for isolating noisy circuit areas is to use a wideband (>100 MHz) oscilloscope with a differential-amplifier front end, as shown in Figure 2. You use the scope to "snoop" along the various circuit paths, looking for noisy elements on the pc board.

Noise appears as a small signal voltage across common-impedance paths, as well as along supply traces. Figure 2 shows the impedance coupling occurs at ground C-B toward ground B-A; ie, noise will likely propagate from package A toward package C.



**FIGURE 1. Common-impedance paths contribute to EMI emissions. They give rise to ground-line voltage drops, as do stray coupling capacitances. The solution? Beef up ground traces; cover the board with them, if possible.**

$V_{CC}$ -supply coupling occurs from package A toward package C. In like manner, coupling occurs from  $V_{CC}$  supplies F to C, E to B and D to A. Check all paths to determine the overall noise level of the circuit layout under maximum clocking conditions and data-transfer rates.

This technique helps you look at the overall qualitative noise level of the pc board and helps isolate areas of potential noise upset. It's not, however, a substitute for the use of a

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qualified EMI facility. Only by rigid testing and measurement under FCC specified conditions can you be assured of EMI-limit certification for electronic equipment.

### Typical Switching Characteristics (Assume 5V at 25°C)

Logic Family	Edge Speed V/NSEC	Input Capacitance (pF)	CdV/dt (mA)
74C/CD4000	0.05	5	0.2
74LS	0.38	6	2.3
74HC	0.42	5	2.1
74S	1.0	4	4.0

#### TRANSITION TIMES AFFECT EMI

The edge rate of an IC's power-supply spike is primarily a function of its signal rise and fall times and its capacitive load, expressed by C(dV/dt). The edge rate is usually expressed in milliamperes per millisecond. For a fixed signal-line or power-supply-trace inductance, the faster the IC's signal rise and fall times, the greater the potential for radiated noise.

The table shows typical speed values for some popular logic families. C(dV/dt) is a measure of the inherent emission behavior—ie, the higher the switching current, the greater the likelihood of noise-energy emission. You can establish a benchmark of the relative emission by taking the edge rate

times the typical input capacitance. As the table shows, HC has a slightly higher edge rate but a slightly lower input capacitance than LS TTL, resulting in a C(dV/dt) figure similar to the latter's.

This conclusion, however, does not take into account other internal spike currents not associated with output loading. These actually increase HC noise slightly. However, HC still achieves approximately the same inherent-noise level as LS TTL, and about 10 times that of CD4000. Don't fall into the trap of believing that because CD4000 and 74C logic use CMOS technology and have low EMI characteristics, HC CMOS logic has low EMI as well.

As seen, the C(dV/dt) figure for the signal lines of 54HC/74HC is about the same as that of LS TTL. Its relative noise is thus about the same. Note that the inherent V<sub>CC</sub> noise generated by high-speed CMOS is somewhat higher than LS TTL's. This is due to the impedance mismatch of the power supply to the IC's supply lines, and to the slightly greater internal spiking in 54HC/74HC circuits. In spite of this higher noise potential, however, proper layout and supply decoupling yield CMOS EMI characteristics similar to those of LS TTL.

An effective method for reducing EMI is to decouple the power supply by adding bypass capacitors between V<sub>CC</sub> and ground. This technique is, of course, closely related to general power-supply decoupling, the goal of which is to maintain correct logic levels. The design of effective decoupling and bypass schemes centers on maximizing the charge stored in circuit bypass loops while minimizing the inductances in these loops.

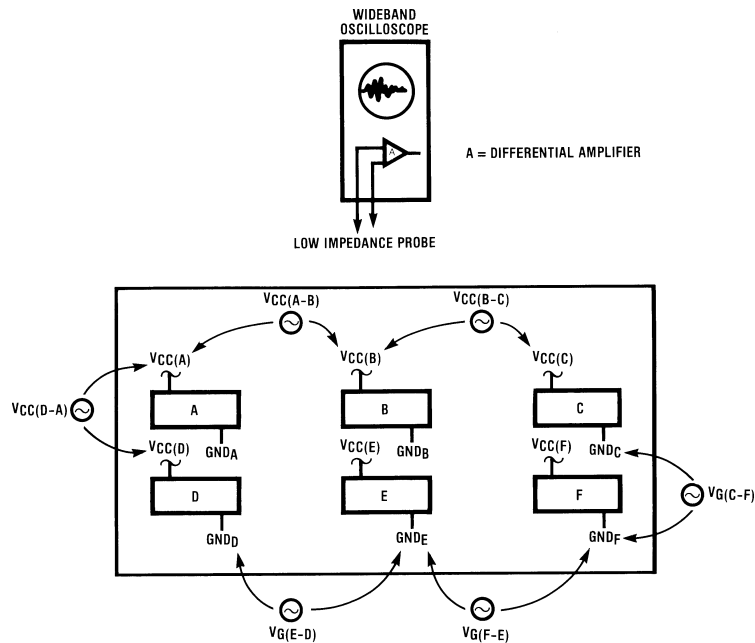


FIGURE 2. This simple setup for evaluating board noise allows you to isolate problem areas qualitatively. The high-speed oscilloscope's differential-amplifier input detects voltage drops along ground and supply lines.

The high decoupling charge levels ensure adequate short-term supply current during supply spiking that's provoked by logic-element switching. Low shunt inductances guarantee minimum voltage drops arising from transients with fast edge rates.

What are the basic requirements for decoupling a power supply? First, you must match the power supply's impedance to that of the individual components. Any power supply presents a low source impedance to other circuitry, whether it be individual components on the same board, or other boards in a multiboard system. These components or boards can comprise logic, memory, microprocessors, analog functions or combinations thereof. You must match the supply's impedance to the components' in order to lessen the potential for voltage drops caused by IC edge rates, ground- or signal-level shifting, noise-induced currents or voltage reflections.

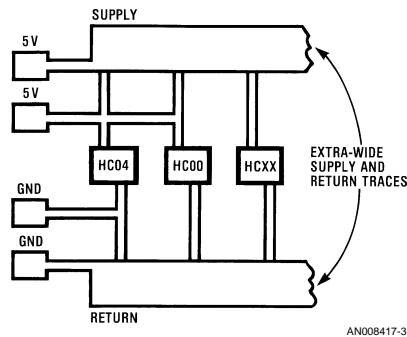
To minimize this mismatch, it's important to use a suitable high-frequency capacitor for bulk decoupling of major circuitry sections, or for entire pc boards in multiboard systems. This capacitor is typically placed at the supply's entry point to the board. It should be an aluminum- or tantalum-electrolytic type having both low equivalent series resistance (ESR) and low equivalent series inductance (ESL). ESR values should range from 1.2 to 4Ω, ESL impedance from 2 to 3Ω (at the system's operating frequency). This capacitor's value is typically 10 to 47 μF. You might additionally need a 0.1 μF high frequency ceramic capacitor if supply noise continues to be a problem.

There exists a second class of decoupling that requires careful examination—that of the ICs themselves. *Figure 4* gives a typical IC's decoupling-circuit model; it shows the parasitic inductances resulting from various lead and trace inductances. The total voltage caused by the switching currents at the IC's pins is the voltage stored in the capacitor,  $V_{CC}$ , minus the drops across the capacitor's ESR and series inductances:

$$V_{IC} = V_{CC} - (I)(ESR) + \frac{dl}{dt} (ESL) + L_L + L_{PC} + L_{IC}$$

Because a capacitor's ESR is typically much smaller than its high-frequency reactance, you can consider the  $(I)(ESR)$  term to be negligible. Rearranging the equation and grouping all inductances together yields

$$V_{IC} = V_{CC} - \frac{dl}{dt} (ESL) + L_{TOTAL}$$



**FIGURE 3. Extra-wide supply and return traces help reduce EMI emissions. Make your boards as “optically opaque” as possible.**

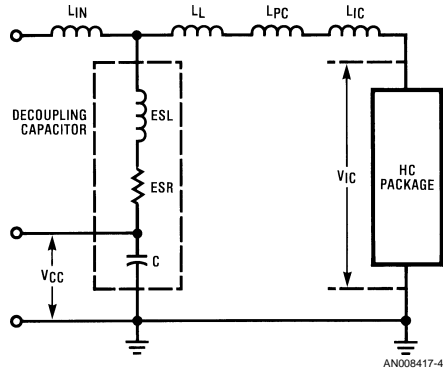
Using this second equation, you can calculate a circuit's maximum allowable decoupling inductance, given the IC's edge rate and the maximum allowable transient voltage drop. This calculation is applicable to general logic-level noise computations as well. For example, for a 500 mV max drop at  $V_{CC} = 5V$  and  $dl/dt = mA/ms$ , the total inductance must not exceed 100 nH. You can then use this calculation to determine the maximum distance between the IC and the bypass capacitor if you know the trace inductance per centimeter.

The foregoing considerations apply to the reduction of noise for suppressing EMI. However, minimizing noise will also help retain maximum logic-level noise immunity. Most popular bipolar-logic families require 0.01- to 0.1 μF RF-grade capacitor placement roughly every two to five packages, depending on the exact application. For high-speed CMOS logic, a good rule of thumb is to place these bypasses every three to five ICs, depending on supply-voltage, operating-speed and EMI requirements. In some cases, moreover, it might be helpful to add 1 μF tantalums at major supply-trace branches, particularly on large pc boards.

In addition to reducing the effects of pc-board trace inductance by bypassing, you should observe careful layout procedures to minimize these inductances. You must therefore maintain the close proximity of ICs and decoupling capacitors. In a specific “how-not-to” example, *Figure 5*: (a) shows

a poor power-rail layout that even the best decoupling capacitor can not clean up; (b) shows the circuit's equivalent series inductances.

In this horror-show scenario, the layout of power-supply and return traces is poor. They're too widely separated, resulting in a large parasitic-antenna loop area, and hence large inductances and much emitted energy. These inductances can result in a significant voltage drop (that the 54HC/74HC logic might tolerate), and they can result in excessive noise generation.



$L_{IN}$  = Total Input Inductance  
 $L_L$  = Total Capacitor-Lead Inductance  
 $L_{PC}$  = Total PC-Board-Trace Inductance  
 $L_{IC}$  = Total IC-Lead Inductance

**FIGURE 4. Decoupling is no simple matter, as borne out by this equivalent circuit. The bypass capacitor's ESR and ESL and the supply line's series inductance all play a detrimental role.**

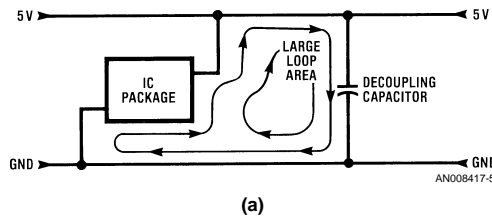
Figure 6 shows methods for reducing the pc-board traces' inductive effects. The power-rail layout in (a) has a low series inductance, thanks to the smaller loop area and the close proximity of the ground and power-supply traces. These factors result in a lower characteristic impedance, which in turn reduces the line-voltage drop. Part (b) shows an alternate orthogonal placement; this geometry results in a similar loop-area reduction (hence EMI reduction), but it needs a greater amount of layout area.

**CONTROLLING IMPEDANCES**

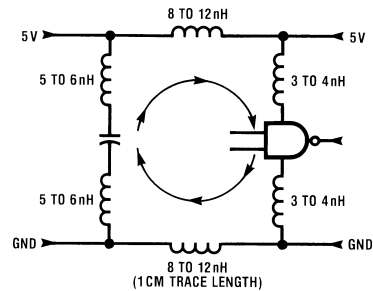
Along with power-supply decoupling, you must consider effective line lengths and terminations in order to reduce noise emission caused by line reflections and mismatch-induced ringing. Because of the fast edge rates discussed earlier, signal-line lengths and transmission-line effects become important factors. When the signal's transit time is greater than the logic's switching time, source and load terminations become critical in long trace runs. A pc board with a dielectric constant of 2 to 3, for example, produces delays of approximately 0.05 ns/cm. To determine the line lengths at which these considerations become important, use the following equation:

$$L < 10 \frac{t_R}{N}$$

where L = interconnect-trace length in centimeters;  $t_R$  = logic rise time in nanoseconds; and N is the number of driven logic inputs. Thus, for a 54HC/74HC logic device driving six other devices, the allowable trace length is  $10(6 \text{ ns})/6 = 10 \text{ cm}$ . This figure represents the maximum allowed trace length to avoid waveform distortion. Implicit in the trace-length calculation is the minimization of pulse reflections, ringing and harmonic generation, which can add to EMI.

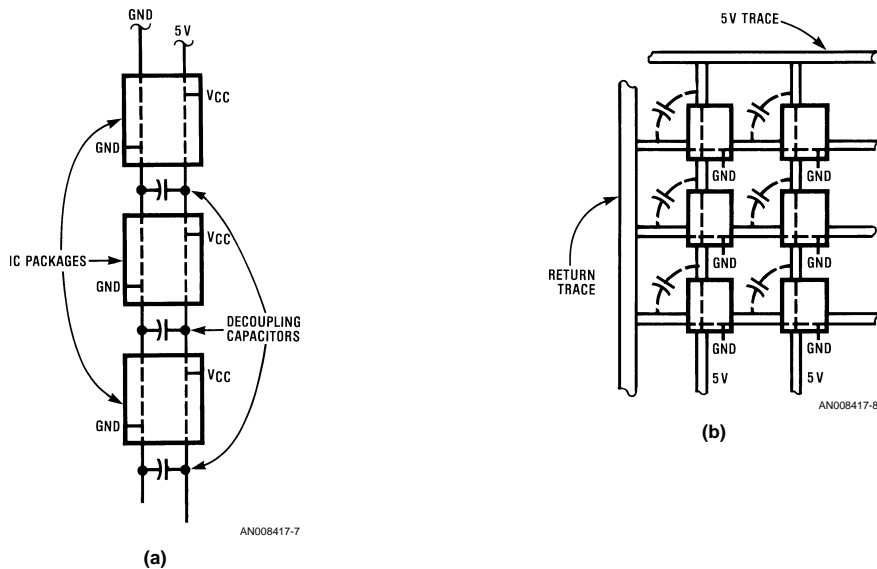


(a)



(b)

**FIGURE 5. This "how-not-to" hookup (a) shows the wrong way to decouple an IC. The layout produces a large loop-antenna area for emitted noise. The equivalent circuit for this configuration is shown in (b).**



**FIGURE 6.** These recommended supply and return layouts help reduce EMI. The reason? They minimize loop area and characteristic impedance, thanks to the proximity of the supply and return lines. The orthogonal arrangement in (b) requires more area than (a)'s lateral layout, but it produces similarly effective results.

#### PLACEMENT IS IMPORTANT

Printed-circuit boards using 54HC/74HC could contain sections of high-speed circuitry combined with sections of low-speed circuitry. *Figure 7* shows the recommended placement of these sections for both single-board (a) and multi-board (b) systems. In the former situation, it's preferable to group all the high-speed circuitry close together. Grouping the system by speed reduces the overall trace lengths in the high-frequency section, which is critical to reducing the overall EMI.

This line-length reduction cuts line reflections, cross-talk, common-impedance coupling and ringing. Note that the higher speed sections are grouped near the power supply as well. The reason? Switching power supplies can be large sources of radiation; external shielding of both the supply and the high-speed circuitry is therefore advisable.

Relative circuit speeds play the important role here. Consequently, the example doesn't give typical values for low, medium or high frequencies. One possible criterion would be to examine the corner frequency or bandwidth of each IC. Also, you must give consideration to IC-interconnection paths. Grouping logic by speed tends to minimize interconnection lengths in general. Depending on the design, however, this point might not be entirely true in some cases.

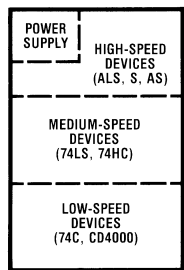
*Figure 7 (b)* shows the grouping of ICs on a pc board used in a multiboard system. In this case, the high-speed circuitry is grouped near the bus connector. The reason for this is that the bus connector usually carries very-high-speed signals; grouping high-frequency circuitry near it minimizes circuit trace lengths. As shown, the lower speed sections are placed further from the edge connector.

#### SHIELD THE SYSTEM

Even though good layout and pc-board design techniques can greatly reduce EMI, in some cases they're not enough; you must shield the internal circuitry to reduce emissions further. The exact design requirements for effective shielding are beyond the scope of this article. However, the topic deserves brief mention. Typically, shielding is accomplished by enclosing the high-speed circuitry in a metal enclosure that has a good earth- and system-ground connection. Ideally, the enclosure completely seals the internal circuitry.

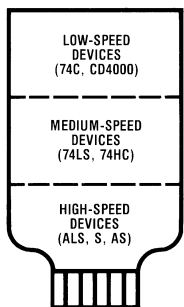
In practice, however, the system enclosure will have "holes" appearing at the places where the system interfaces to the real world. For example, a display, keyboard or disk drive might require enclosure cutouts to allow cables to enter the system's box. Moreover, vents and fans might be required for cooling.

It's important in critical situations to minimize these holes. In this respect, 54HC/74HC has an advantage over other logic families. Thanks to its lower power consumption, you can in many cases eliminate vents and fans, and thus seal the enclosure more effectively.



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(a)



AN008417-13

(b)

**FIGURE 7. Grouping ICs by frequency can help. In (a)'s single-board layout, the high-speed circuitry is placed closest to the power supply. In (b)'s multiboard system, the high-speed units are the closest to the board connector.**

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