

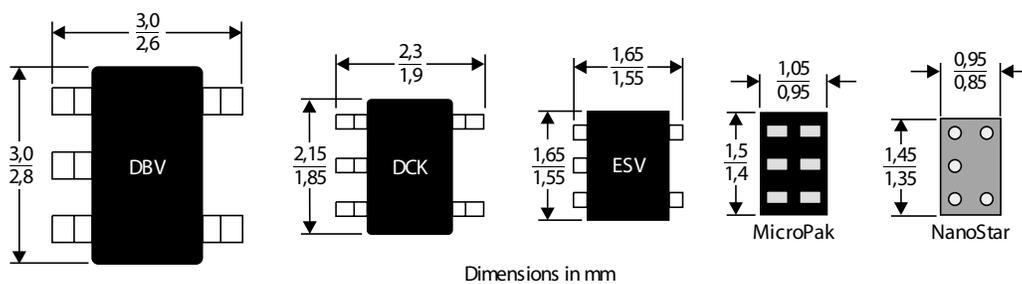
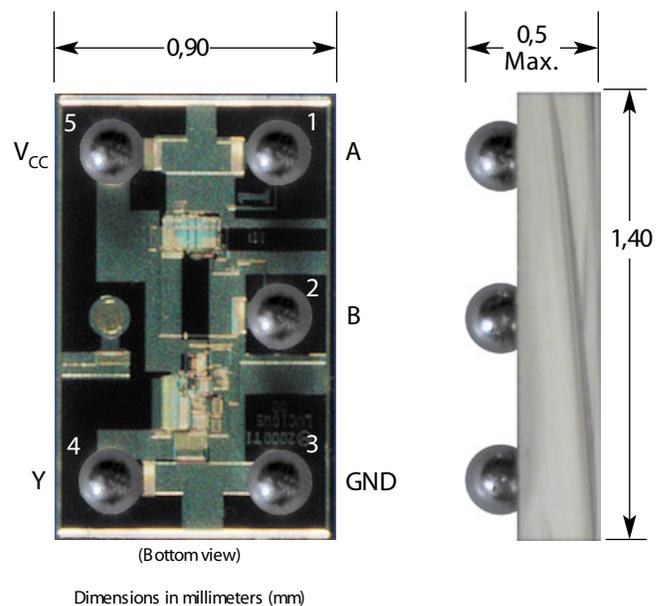
Design Summary for NanoStar™ Little Logic

www.ti.com/sc/nanostar



Introduction to NanoStar Little Logic

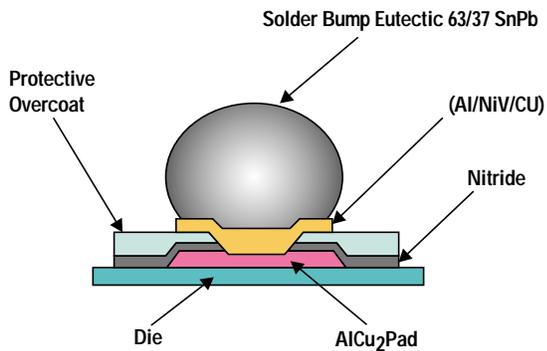
Texas Instruments (TI) now offers the smallest single gate logic family available. NanoStar Little Logic consists of single gate logic functions packaged in a chip scaled package. NanoStar Little Logic reduces board space requirements several times over the conventional 5-pin package. This micro scale technology is driven by applications requiring a very small circuit board mounting area. The NanoStar Little Logic family offers the most popular logic functions for space-constrained systems such as cellular phones, pagers, and portable consumer products (Cellular, DVD/CD ROMs, MD/MP3/CD players, VCRs, Digital Video Camcorders, Digital STB, DSC, notebook computers, PC cards, and Personal Digital Assistants). They can also be used as simple glue/repair logic to implement last minute design changes or to eliminate dependence on intricate line layout patterns and simplify routing. TI provides Little Logic functions in the LVC, AHC and AHCT families. The technology used is a major breakthrough in IC packaging concepts, using the die as the package. Space savings can be compared below.



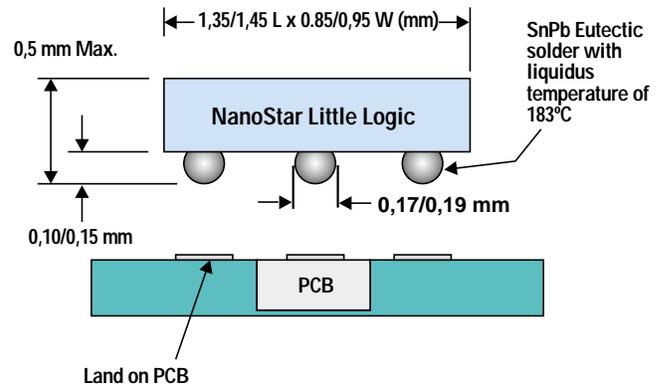
	SOT-23 (DBV) (TI)	SC-70 (DCK) (TI)	ESV	MicroPak™	NanoStar™ (YEA)
Length (mm)	2,90 ± 0,1	2,00 ± 0,15	1,60 ± 0,05	1,45 ± 0,05	1,40 ± 0,05
Width (mm)	2,80 ± 0,2	2,10 ± 0,2	1,60 ± 0,05	1,00 ± 0,05	0,90 ± 0,05
Height (mm)	1,20	0,95	0,55	0,55	0,50
Footprint Area (mm²)	8,12	4,20	2,56	1,45	1,26
Weight (gm)	0,0135	0,006	0,003	0,001	0,001

PCB Design Guidelines

Solder Ball Composition

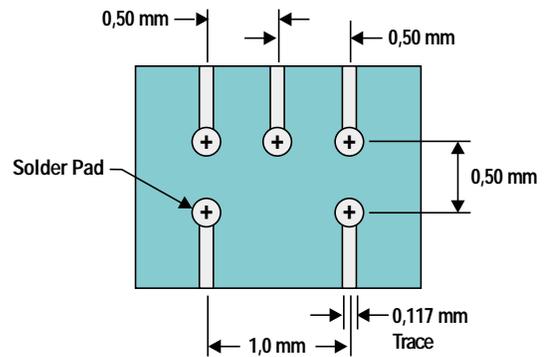
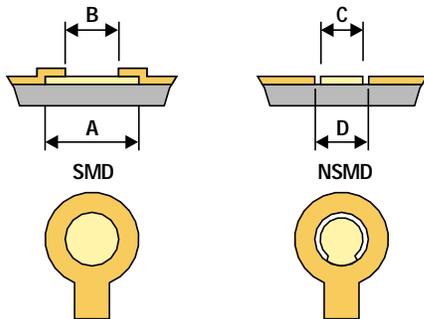


Package Configuration (0,5-mm Ball Pitch) Jedec MO-211 pending



Note: Self-planarizing package.

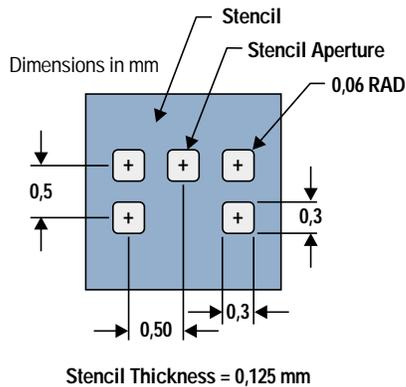
Solder Mask and Non-Solder Mask



The PCB layout assumes 0,117-mm (4.6-mil) trace width and 1-oz. copper layer thickness.

Solder Mask Defined (SMD) Pad		Non-Solder Mask Defined (NSMD) Pad Preferred	
Copper Pad	Solder Mask Opening	Copper Pad	Solder Mask Opening
"A"	"B"	"C"	"D"
0,350 mm ±0,025 (13.8 mils)	0,175 mm ±0,025 (6.9 mils)	0,175mm +0,000/-0,025 (6.9 mils)	0,350 mm ±0,025 (13.8 mils)

Stencil Vitals



Solder Paste

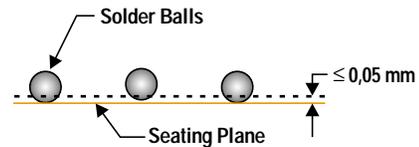
TI recommends the use of type 3 or finer solder paste when mounting the NanoStar package. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted components.

Geometric Dimensional Tolerances

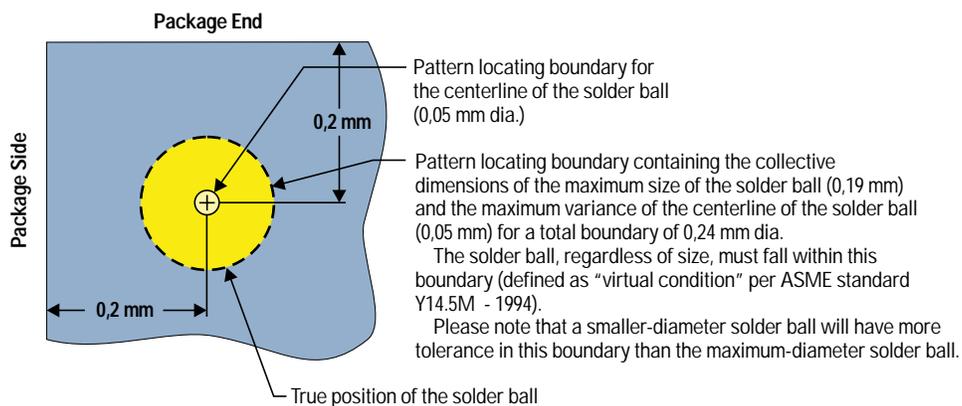
Coplanarity

This package meets a coplanarity of 0,05 mm as shown. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5M - 1994)



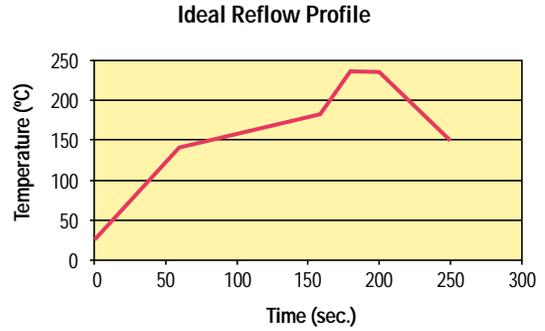
Position Tolerance

A graphic representation is shown below for the top, left solder ball of the NanoStar package.



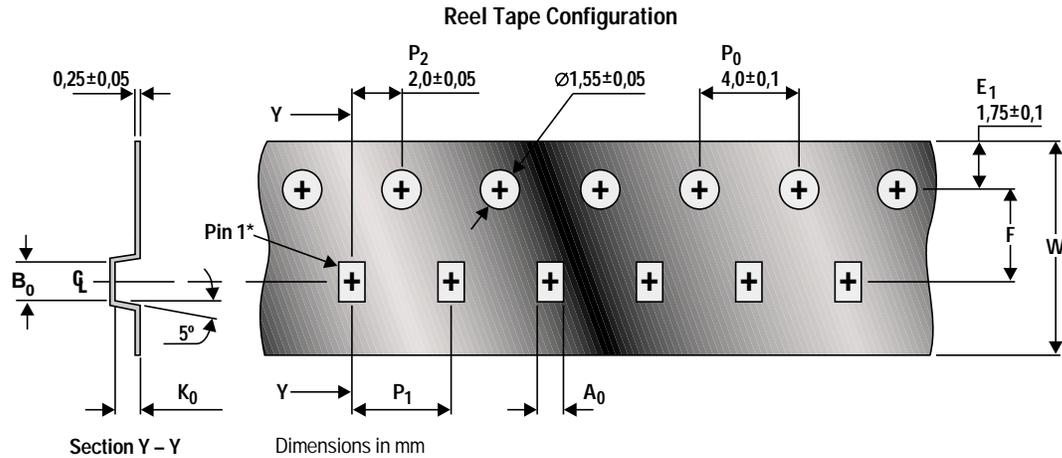
IR Reflow Profile

Ideal (1st and 2nd) Reflow Profile	
RT to 140°C	60 – 90 sec.
140°C to 180°C	60 – 120 sec.
Time Above 183°C	60 – 150 sec.
Peak Temp.	220°C ±5°C
Time Within 5°C Peak Temp.	10 – 20 sec.
Ramp Down Rate	6°sec. Max.



Note: This is an ideal profile, and actual conditions obtained in any specified reflow oven will vary. This profile is based on convection or RF plus forced convection heating.

Packaging Tape and Reel



Cover Tape Width (W)	Pocket Pitch (P ₁)	Reel Width	Reel Dia.	Pocket Width (A ₀)	Pocket Length (B ₀)	Pocket Depth (K ₀)	Hole to Pocket CL (P ₂)	Hole to Pocket CL (F)	Sprocket Hole Pitch (P ₀)
8,00 ± 0,3	4,00 ± 0,1	8,0 +2,0/-0	330 max	1,10 ± 0,05	1,60 ± 0,05	0,56 ± 0,05	2,0 ± 0,05	3,5 ± 0,05	4,0 ± 0,1

Sockets

Socket & Socket Manufacturer (Ordering Information)

Socket Number: 02-9023

Everett Charles Technologies

4837 White Bear Parkway

St. Paul, MN 55110

Ph: 651-407-7777

FAX: 651-407-7290

Web Address: www.ectinfo.com

Electrical Characteristics

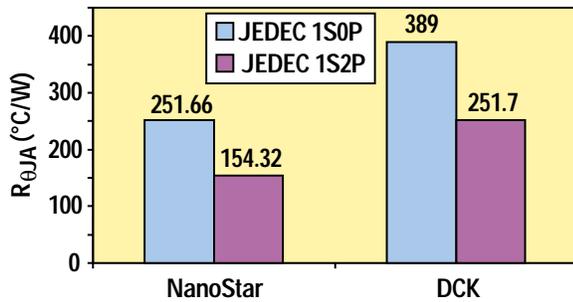
	R (ohms)	L (nH)	C (pF)
Min.	0.001	0.021	0.045
Mean	0.001	0.021	0.046
Max.	0.001	0.021	0.047

Note: Electrical package parasitic was achieved through PACED electrical modeling and is based on a 3D model. Actual electrical data may differ slightly from simulated results.

Parameter Name	LVC1GxxYEA
Voltage Nodes (V)	5, 3.3, 2.5, 1.8
V _{CC} Range (V)	1.65 to 5.5
Input Level	CMOS
Output Level	CMOS
Output Drive (mA)	(-4/4, -8/8, -16/16, -24/24, -32/32)
No. of Gates	1
Static Current (mA)	0.01
t _{pd} (max) (ns)	9.9

Thermal Characteristics

Comparison of NanoStar and DCK Thermal Impedance



JEDEC 1S2P	Airflow (linear ft/minute)			
	0	150	250	500
NanoStar				
R _{θJA} (° C/W)	154.32	152.05	150.73	148.72
R _{θJC} (° C/W)	18.72			
DCK				
R _{θJA} (° C/W)	251.7	250.1	247.2	242.7
R _{θJC} (° C/W)	144.4			

Board Level Reliability Data

Board Level Reliability N _f (cycles to 1.0% failure)	
NanoStar	1150 cycles

Note: Board level reliability data was achieved through Finite Element Modeling of actual package construction and is based on the PCB pad finish being Copper (OSP). Actual reliability data may differ slightly from simulated results.

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	Domestic	0120-81-0036
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	Domestic	www.tij.co.jp/pic

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	Singapore	800-0111-111	-800-800-1450
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