

Using Schmitt Triggers for Low Slew-Rate Input

Introduction

Actel's SX-A and SX-S device families are designed to accommodate a variety of I/O standards. This allows users to easily integrate these FPGAs with other devices that have adopted a compatible I/O standard. In order to achieve this I/O flexibility as well as higher device performance, SX-A and SX-S devices use smaller device geometries. As a result, slow input signals with low slew rates, such as board power-on-resets or waveforms generated by a crystal oscillator, may be prone to functional failures in these devices. One approach for negating low slew-rate effects is the use of a Schmitt-trigger buffer applied at the input to the FPGA. This document discusses in detail the input slew-rate characteristics of the SX-A and SX-S devices and how the use of Schmitt triggers can aid in low slew-rate applications.

Background

An ideal input signal is an instantaneous transition from logic low to logic high or vice versa (Figure 1). However, inherent parasitic capacitance, resistance, and inductance in the input path and input buffer cause an input signal to have a finite amount of rise or fall time (Figure 2). This time is referred to as slew rate and is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing.

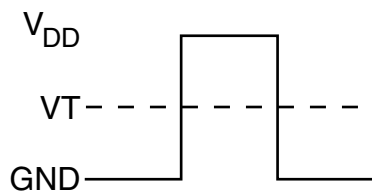


Figure 1 • Ideal Input Transfer

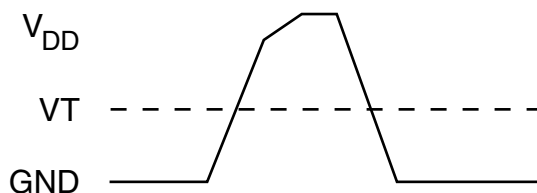


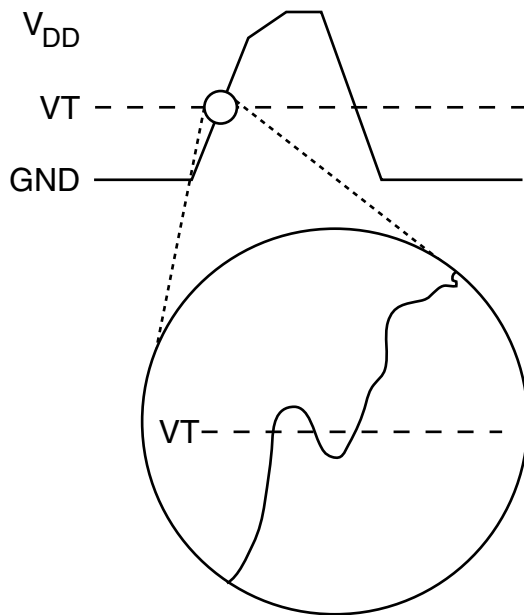
Figure 2 • Realistic Input Transfer

In certain applications, a user may require a very fast (i.e. high slew rate) signal, which approaches an ideal switching transition. This can be accomplished by reducing the track resistance and/or capacitance on the board or by increasing the drive capability of the input signal. Both of these options are generally time consuming and costly. Furthermore, the closer the input signal approaches an ideal one, the greater the likelihood of unwanted effects such as increased peak current, capacitive coupling, and ground bounce. In many cases, a designer might want to incorporate a finite amount of slew rate into their signal in order to reduce these effects.

On the other hand, if an input signal becomes too slow (i.e. low slew rate), then noise around the FPGA's input voltage threshold can cause multiple state changes (Figure 3 on page 2). During the transition time, both input buffer transistors could potentially turn on at the same time. This could cause two major consequences. In the worst case event, this might damage the device. A second, less catastrophic scenario, could result in the output of the buffer to oscillating unpredictably. In this situation, the input buffer could still pass signals. However, these short, unpredictable oscillations would surely cause the device to malfunction.

For example, many board designers use a crystal oscillator to generate a high-frequency clock signal that drives a number of devices on the board. Due to the nature of crystal oscillator circuits, the generated clock signal may exhibit low slew rate. As this clock signal approaches the FPGA input threshold voltage, noise concerns could cause multiple state changes to occur at the clock input pin (Figure 3 on page 2). Consequently, registers would latch information prematurely and most likely result in functional failures at the output pins of the FPGA.

Another complication of low slew-rate signals is timing concerns. For instance, many board designers use "power-on-reset" circuitry to reset every chip on a board into a pre-defined state. The resulting large utilization of board-level routing resources increases parasitic effects, results in a very low slew rate on the reset signal. A poorly designed board could run into problems if the threshold voltage on the FPGA reset pin is not reached before asserting the other functional inputs. In this situation, the FPGA may be reset at unwanted times.



Like any other integrated circuit, both SX-A and SX-S devices can be affected by the low slew-rate problems mentioned earlier. [Table 1](#) and [Table 2](#) outline the absolute minimum slew-rate values for the each of the different I/O standards supported by these devices. The numbers listed in these tables are based on rise/fall times between the 10% and 90% voltage points collected in a lab environment at room temperature. Therefore, the worst case values are not guaranteed.

Figure 3 • *Multiple State Changes at the Input Threshold Level*

Table 1 • *SX-A Device Family Minimum Input Slew Rate*

| Rise time | | | | | |
|------------|------------|-----------|-----------|------------|-----------|
| I/O Buffer | PCI | | TTL | | |
| | 3.3V | 5.0V | 2.5V | 3.3V | 5.0V |
| Inbuf | 176 mV/ns | 222 mV/ns | 133 mV/ns | 176 mV/ns | 160 mV/ns |
| Clkbuf | 10.5 mV/ns | 16 mV/ns | 8 mV/ns | 10.5 mV/ns | 16 mV/ns |
| Hclkbuf | 14.7 mV/ns | 27 mV/ns | 8 mV/ns | 14.7 mV/ns | 27 mV/ns |
| Fall time | | | | | |
| I/O Buffer | PCI | | TTL | | |
| | 3.3V | 5.0V | 2.5V | 3.3V | 5.0V |
| Inbuf | 63 mV/ns | 93 mV/ns | 38 mV/ns | 75 mV/ns | 133 mV/ns |
| Clkbuf | 10.5 mV/ns | 16 mV/ns | 8 mV/ns | 10.5 mV/ns | 16 mV/ns |
| Hclkbuf | 14.7 mV/ns | 27 mV/ns | 8 mV/ns | 14.7 mV/ns | 27 mV/ns |

Table 2 • SX-S Device Family Minimum Input Slew Rate

| rise time | | | | | |
|------------|------------|-----------|------------|------------|-----------|
| I/O Buffer | PCI | | TTL | | CMOS |
| | 3.3V | 5.0V | 3.3V | 5.0V | 5.0V |
| Inbuf | 176 mV/ns | 222 mV/ns | 133 mV/ns | 176 mV/ns | 160 mV/ns |
| Clkbuf | 10.5 mV/ns | 16 mV/ns | 8 mV/ns | 10.5 mV/ns | N/A |
| Hclkbuf | 14.7 mV/ns | 27 mV/ns | 14.7 mV/ns | 27 mV/ns | N/A |
| Qclkbuf | 10.5 mV/ns | 16 mV/ns | 8 mV/ns | 10.5 mV/ns | N/A |
| fall time | | | | | |
| I/O Buffer | PCI | | TTL | | CMOS |
| | 3.3V | 5.0V | 3.3V | 5.0V | 5.0V |
| Inbuf | 63 mV/ns | 93 mV/ns | 75 mV/ns | 133 mV/ns | 62 mV/ns |
| Clkbuf | 10.5 mV/ns | 16 mV/ns | 8 mV/ns | 10.5 mV/ns | N/A |
| Hclkbuf | 14.7 mV/ns | 27 mV/ns | 14.7 mV/ns | 27 mV/ns | N/A |
| Qclkbuf | 10.5 mV/ns | 16 mV/ns | 8 mV/ns | 10.5 mV/ns | N/A |

Using Schmitt-Trigger Buffers to Reduce the Slew Rate

One way to eliminate problems with low slew rate is with Schmitt triggers. A Schmitt trigger is a buffer used to convert a slow or noisy signal into a clean one before passing it to the FPGA. This is a simple, low-cost solution for a user working with low slew-rate signals.

Schmitt-trigger buffers have a transfer function with hysteresis. Figure 4 shows a hysteresis curve where the input voltage is on the x-axis and the output voltage is on the y-axis. As the input voltage rises from 0V towards 1.7V, the output will remain at 0 volts. Only when the input exceeds 1.7V will the output jump up to 5V. At this point, reducing the input voltage will not cause the output to drop to zero immediately. This only happens when the input voltage is reduced to 0.9V. One can see that the input level at which the output increases to maximum and the level at which it drops to minimum are different. This characteristic is known as hysteresis.

If we apply the hysteresis theory to the noisy signal shown in Figure 5, one will notice that an almost perfect output is recovered from a slow and very noisy input.

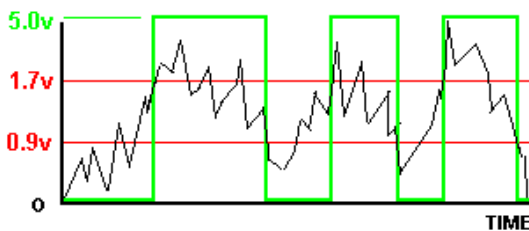


Figure 5 • Applying Noisy Input to a Schmitt-Trigger Buffer

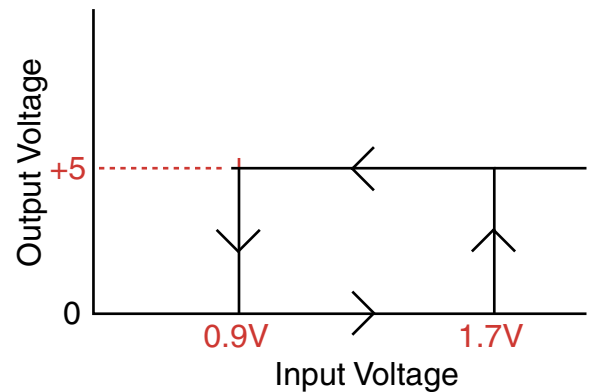


Figure 4 • Ideal Hysteresis Curve of Schmitt-Trigger Buffer

Schmitt triggers utilize the hysteresis phenomena with two voltage thresholds. An upper threshold is used to generate an output transition as the input switches from low to high, and a lower threshold is used to generate an output transition as the input switches from high to low. Such a trigger scheme is highly resistant to noise as long as the peak-to-peak amplitude of the noise is less than the difference between the threshold voltages (i.e. less than $1.7 - 0.9 = 0.8V$). Similarly, a low slew-rate signal turns into a sharp, high slew-rate signal after passing through a Schmitt-trigger buffer as shown in Figure 6 on page 4.

Schmitt triggers can be easily incorporated into a design with minimal performance cost. Actel recommends that a Schmitt trigger be used to buffer a signal if input slew rates fall below the values outlined in specification for SX-A and SX-S devices.

Depending on the application, different Schmitt-trigger buffers can be used to fulfill the requirements. Schmitt-trigger buffers are categorized in three configurations:

- Fixed threshold voltages with non-inverted outputs
- Fixed threshold voltages and inverted outputs
- Variable threshold voltages with non-inverted outputs

Device 74HC14 is a Schmitt-trigger buffer with fixed threshold voltages and an inverted output. Due to the simple circuit design, the 74HC14 is one of the most popular devices for interfacing real-world signals to digital electronics. A little-known fact about the 74HC14 is that using negative feedback from output to input can alter the thresholds. For example, adding a $5.1\text{M}\Omega$ resistor from output to input and a $1\text{M}\Omega$ input resistor provides negative feedback of about 15%. That is subtracted from the internal 30% positive feedback and, with $V_{CC}=5\text{V}$, it effectively changes the lower and upper thresholds at the input of the $1\text{M}\Omega$ resistor to approximately 2.1V and 2.9V, respectively. This is very useful if the signal of interest has smaller transitions than the normal 74HC14 hysteresis voltage.

Beside the 74HC14, there are a number of different ways to implement a Schmitt trigger in CMOS logic. The simplest is to use a non-inverting buffer and connect a $3\text{M}\Omega$ resistor from output to input to provide positive feedback, which is summed with the input signal through a $1\text{M}\Omega$ series resistor. This scheme is shown in part a of [Figure 7 on page 5](#). These resistor values will give the same thresholds as a 74HC14, but keep in mind that the input resistance is $4\text{M}\Omega$ to either GND or V_{CC} , depending on the current output status.

The same functionality can be achieved with two inverters (like the 74HC240) as shown in part b of [Figure 7 on page 5](#). In this configuration, both inverted and non-inverted signals are available to the FPGA.

Op-amp buffers can also be used to implement simple Schmitt-trigger buffers. Two Op-amp-based Schmitt-trigger buffers are shown in [Figure 8 on page 5](#). As indicated in [Figure 8 on page 5](#), the polarity of the inputs to the op-amp can be used to generate an inverted or non-inverted output. Furthermore, the threshold and hysteresis can be adjusted by trial and error.

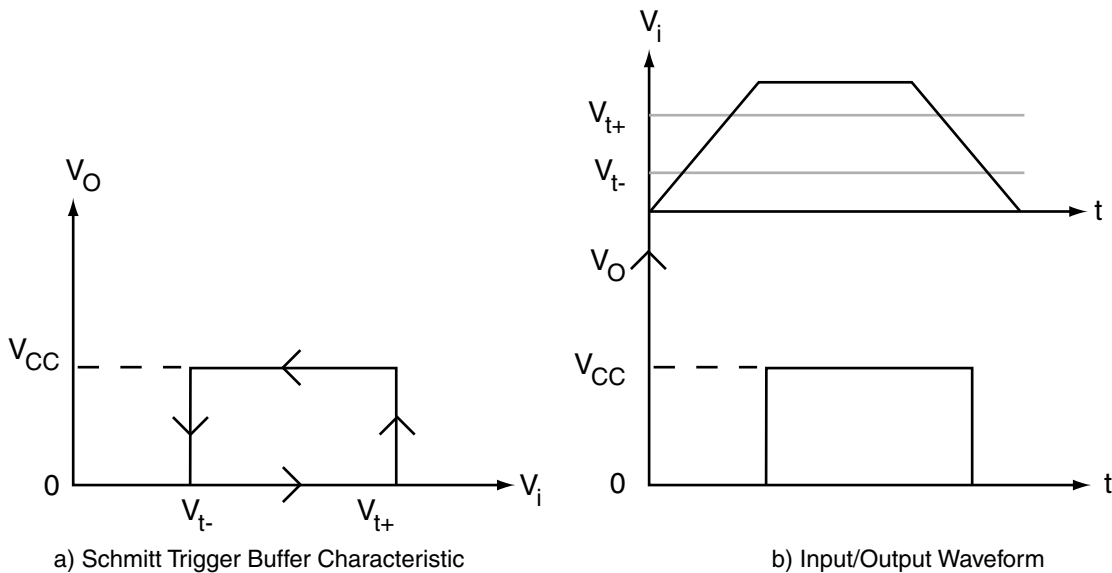


Figure 6 • *Applying a Low Slew-Rate Input to a Schmitt-Trigger Buffer*

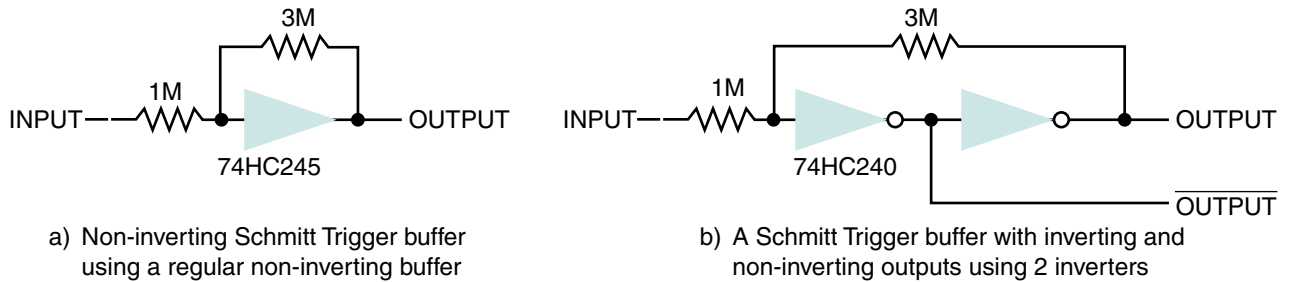


Figure 7 • Schmitt-Trigger Buffers Using Inverters

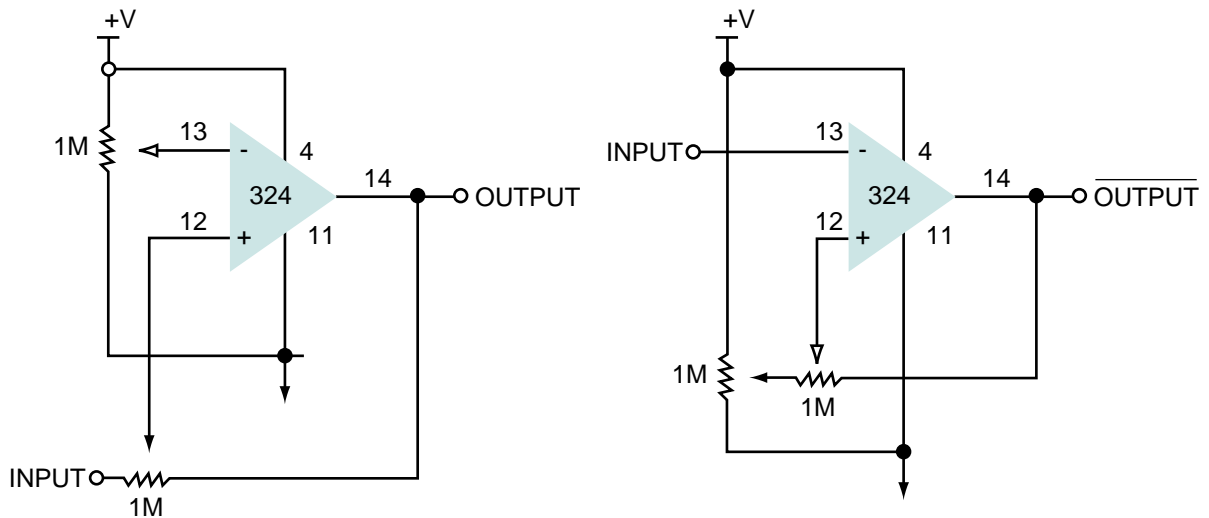


Figure 8 • Schmitt-Trigger Buffers Using OPAMPs

Conclusion

Actel's SX-A and SX-S families have been designed for optimal performance, minimal power penalty, and very high reliability. They have always been an excellent solution for both commercial and military applications. In addition, with the aid of Schmitt-trigger buffers, low slew-rate applications can also be handled with ease. Implementation of these buffers is simple, not expensive, and flexible in terms that different configurations are possible depending on the application. The characteristics of Schmitt-trigger buffers (e.g. threshold voltage) can be fixed or user-adjustable if required. Using Schmitt-trigger buffers guarantees a fast, noise-free, input signal to the FPGA.

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