

# I/O PORTS

## P89LPC933/934/935

## 5. I/O PORTS

The **P89LPC933/934/935** has 4 I/O ports: Port 0, Port 1, Port2, and Port 3. Ports 0, 1, and 2 are 8-bit ports and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen (see Table 5-1).

**Table 5-1: Number of I/O pins available.**

Clock source	Reset option	Number of I/O pins
		28-pin package
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported	23

### Port configurations

All but three I/O port pins on the **P89LPC933/934/935** may be configured by software to one of four types on a bit-by-bit basis, as shown in Table 5-2. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ( $\overline{\text{RST}}$ ) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$ ) may only be configured to be either input-only or open drain.

**Table 5-2: Port output configuration settings**

PxM1.y	PxM2.y	Port output mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

### Quasi-bidirectional output configuration

Quasi-bidirectional outputs can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

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The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for two CPU clocks quickly pulling the port pin high.

The quasi-bidirectional port configuration is shown in Figure 5-1.

Although the **P89LPC933/934/935** is a 3 V device most of the pins are 5 V-tolerant. If 5 V is applied to a pin configured in quasi-bidirectional mode, there will be a current flowing from the pin to  $V_{DD}$  causing extra power consumption. Therefore, applying 5 V to pins configured in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

(Please refer to the **P89LPC933/934/935** datasheet, AC Electrical Characteristics for glitch filter specifications)

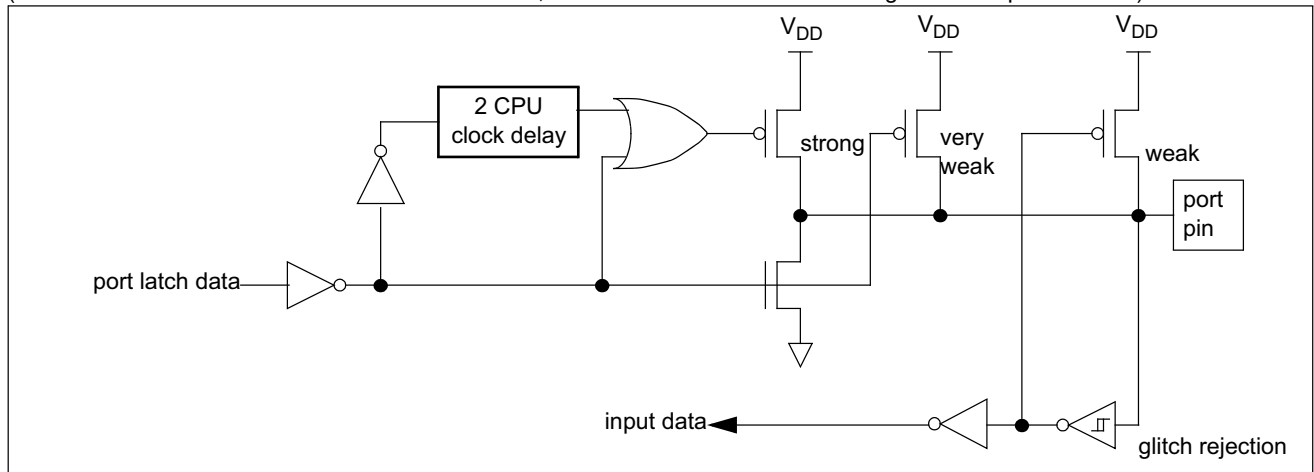


Figure 5-1: Quasi-bidirectional output

### Open drain output configuration

The open drain output configuration turns off all pull-ups and only drives the pulldown transistor of the port pin when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to  $V_{DD}$ . The pulldown for this mode is the same as for the quasi-bidirectional mode.

The open drain port configuration is shown in Figure 5-2.

An open drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

Please refer to the **P89LPC933/934/935** datasheet, AC Electrical Characteristics for glitch filter specifications).

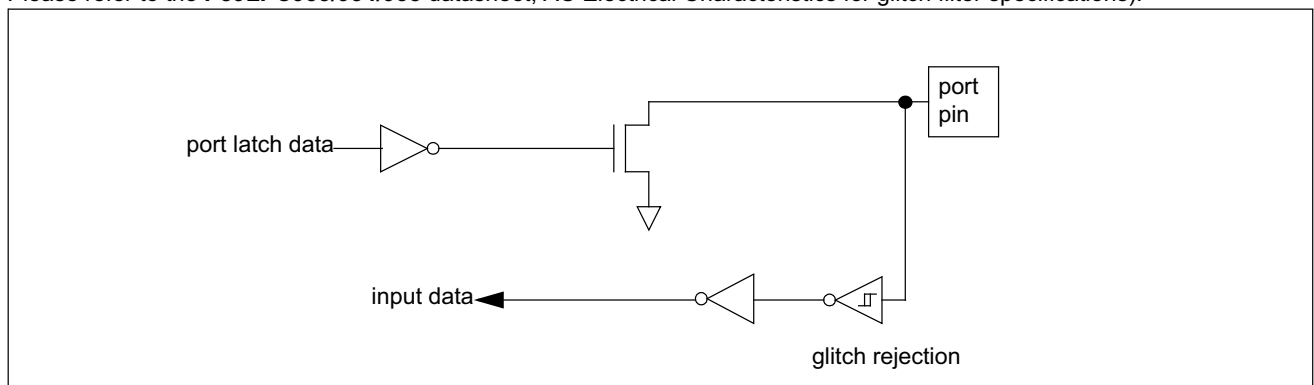


Figure 5-2: Open drain output

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### Input-only configuration

The input port configuration is shown in Figure 5-3. It is a Schmitt-triggered input that also has a glitch suppression circuit.

(Please refer to the **P89LPC933/934/935** datasheet, AC Electrical Characteristics for glitch filter specifications)

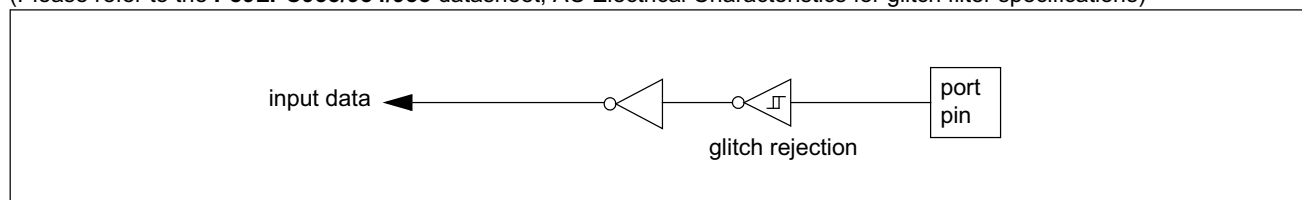


Figure 5-3: Input -only

### Push-pull output configuration

The push-pull output configuration has the same pulldown structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output.

The push-pull port configuration is shown in Figure 5-4.

A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

(Please refer to the **P89LPC933/934/935** datasheet, AC Electrical Characteristics for glitch filter specifications)

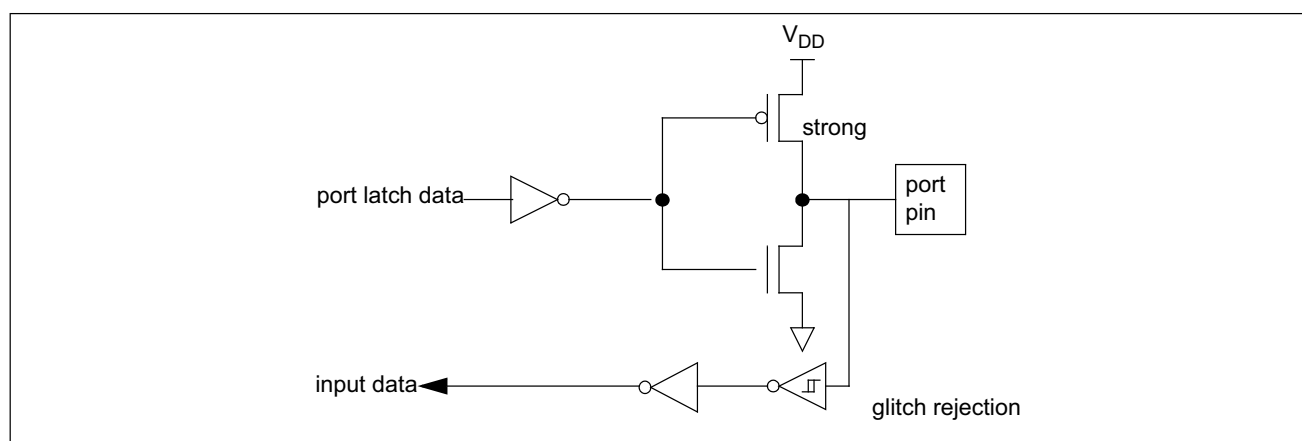


Figure 5-4: Push-pull output

### Port 0 and Analog Comparator functions

The **P89LPC933/934/935** incorporates two Analog Comparators. In order to give the best analog performance and minimize power consumption, pins that are being used for analog functions must have both the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port pins into the input-only mode as described in the Port Configurations section (see Table 5-2).

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. Bits 1 through 5 in this register correspond to pins P0.1 through P0.5 of Port 0, respectively. Setting the corresponding bit in PT0AD disables that pin's digital input. Port bits that have their digital inputs disabled will be read as 0 by any instruction that accesses the port.

On any reset, PT0AD bits 1 through 5 default to '0's to enable the digital functions.

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### I/O pins used with ADC functions

The **P89LPC933/934/935** incorporates two A/D converters. In order to give the best analog performance pins that are being used with the ADC should have their digital outputs and inputs disabled and have the 5V tolerance disconnected. Digital outputs are disabled by putting the port pins into the input-only mode as described in the Port Configurations section (see Table 5-2). Digital inputs will be disconnected automatically provided that the corresponding ADC is enabled and the corresponding bit in the ADINS register has been set.

**Table 5-3: Port output configuration**

Port pin	Configuration SFR bits		Alternate usage	Notes
	PxM1.y	PxM2.y		
P0.0	P0M1.0	P0M2.0	KBI0,CMP2, AD01	Refer to section "Port 0 and Analog Comparator functions" for usage as analog inputs (CIN2B, CIN2A, CIN1B, CIN1A and CMPREF)
P0.1	P0M1.1	P0M2.1	KBI1,CIN2B, AD10	
P0.2	P0M1.2	P0M2.2	KBI2,CIN2A, AD11	
P0.3	P0M1.3	P0M2.3	KBI3,CIN1B, AD12	
P0.4	P0M1.4	P0M2.4	KBI4,CIN1A, AD13, DAC1	
P0.5	P0M1.5	P0M2.5	KBI5,CMPREF	
P0.6	P0M1.6	P0M2.6	KBI6,CMP1	
P0.7	P0M1.7	P0M2.7	KBI7,T1	
P1.0	P1M1.0	P1M2.0	TxD	
P1.1	P1M1.1	P1M2.1	RxD	
P1.2	P1M1.2	P1M2.2	T0,SCL	input-only or open-drain
P1.3	P1M1.3	P1M2.3	INT0,SDA	input-only or open-drain
P1.4	P1M1.4	P1M2.4	INT1	
P1.5	not configurable		RST	Input only. Usage as general purpose input or RST is determined by User Configuration Bit RPD (UCFG1.6). Always a reset input during a power-on sequence.
P1.6	P1M1.6	P1M2.6	OCB	
P1.7	P1M1.7	P1M2.7	OCC, AD00	
P2.0	P2M1.0	P2M2.0	ICB, AD03, DAC0	
P2.1	P2M1.1	P2M2.1	OCD, AD02	
P2.2	P2M1.2	P2M2.2	MOSI	
P2.3	P2M1.3	P2M2.3	MISO	
P2.4	P2M1.4	P2M2.4	SS	
P2.5	P2M1.5	P2M2.5	SPICLK	
P2.6	P2M1.6	P2M2.6	OCA	
P2.7	P2M1.7	P2M2.7	ICA	
P3.0	P3M1.0	P3M2.0	XTAL2,CLKOUT	
P3.1	P3M1.1	P3M2.1	XTAL1	

### Additional port features

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After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open drain.

Every output on the **P89LPC933/934/935** has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to the **P89LPC933/934/935** Datasheet for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.