

Instead, if the WDT is used to generate interrupts the current is reduced to approximately 50  $\mu$ A. Whenever the WDT underflows, the device will wake-up.

## 17. Additional features

The AUXR1 register contains several special purpose control bits that relate to several chip features. AUXR1 is described in [Table 106](#)

**Table 105: AUXR1 register (address A2h) bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS
Reset	0	0	0	0	0	0	x	0

**Table 106: AUXR1 register (address A2h) bit description**

Bit	Symbol	Description
0	DPS	Data Pointer Select. Chooses one of two Data Pointers.
1	-	Not used. Allowable to set to a logic 1.
2	0	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
3	SRST	Software Reset. When set by software, resets the P89LPC933/934/935/936 as if a hardware reset occurred.
4	ENT0	When set the P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate. Refer to <a href="#">Section 8 "Timers 0 and 1"</a> for details.
5	ENT1	When set, the P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate. Refer to <a href="#">Section 8 "Timers 0 and 1"</a> for details.
6	EBRR	UART Break Detect Reset Enable. If logic 1, UART Break Detect will cause a chip reset and force the device into ISP mode.
7	CLKLP	Clock Low Power Select. When set, reduces power consumption in the clock circuits. Can be used when the clock frequency is 8 MHz or less. After reset this bit is cleared to support up to 12 MHz operation.