- ◆ Basic Block Diagram
- diagram operation

- ◆ Basic Block Diagram
- diagram operation
- Phase Detector

- ◆ Basic Block Diagram
- diagram operation
- Phase Detector
- xor CD4046 phase II

- ◆ Basic Block Diagram
- diagram operation
- Phase Detector
- ◆ xor CD4046 phase II
- ◆ Loop Filter

- ◆ Basic Block Diagram
- diagram operation
- Phase Detector
- ◆ xor CD4046 phase II
- Loop Filter
- VCO

inputs:NI & INV

input & feedback

♦ inputs:NI & INV

output: voltage

input & feedback

freq (or phase)

- ◆ inputs:NI & INV
- ◆ output: voltage
- \bullet -fb $=>V_{INV}=V_{NI}$

input & feedback

freq (or phase)

$$-fb \Rightarrow f_{fb} = f_{in}$$

- ◆ inputs:NI & INV
- ◆ output: voltage
- \bullet -fb $=> V_{INV} = V_{NI}$
- v = volt x

input & feedback

freq (or phase)

$$-fb => f_{fb} = f_{in}$$

freq div => freq x

- ◆ inputs:NI & INV
- ◆ output: voltage
- lacktriangle -fb \Rightarrow $V_{INV} = V_{NI}$
- \bullet v div in -fb => volt x
- very robust wrt V
 - self correcting

input & feedback

freq (or phase)

$$-fb \Rightarrow f_{fb} = f_{in}$$

freq div => freq x

very robust wrt f

self correcting

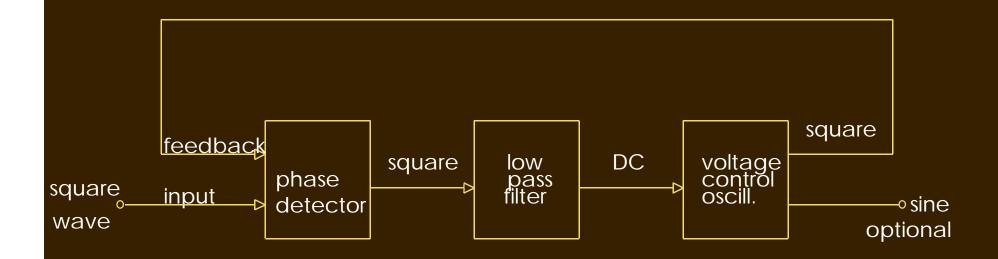
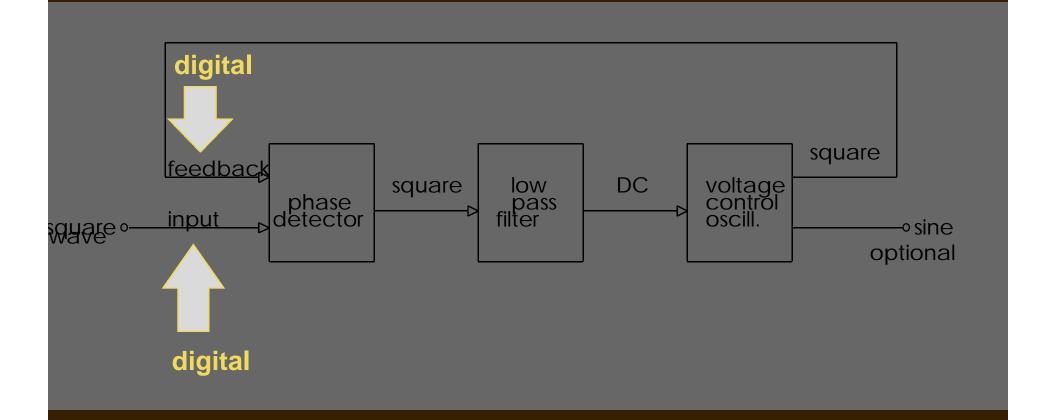
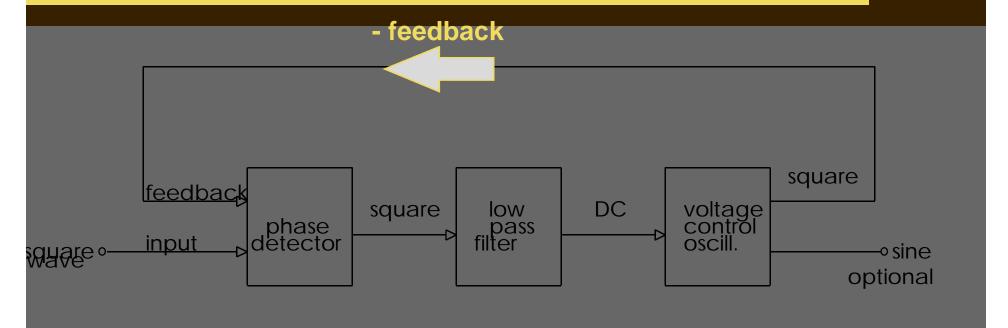
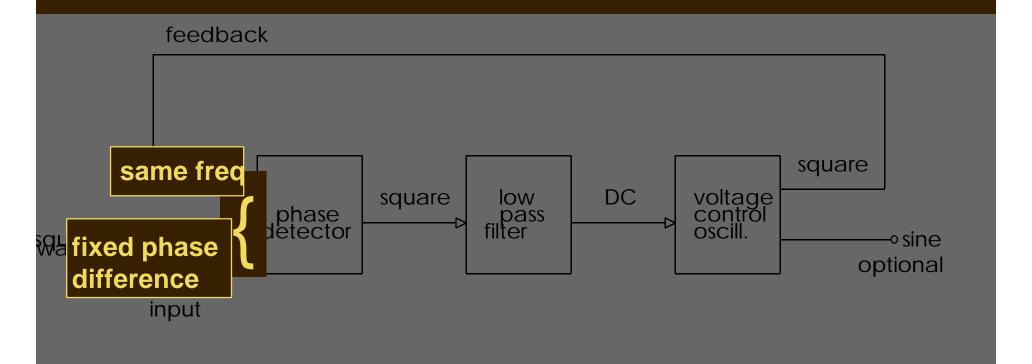
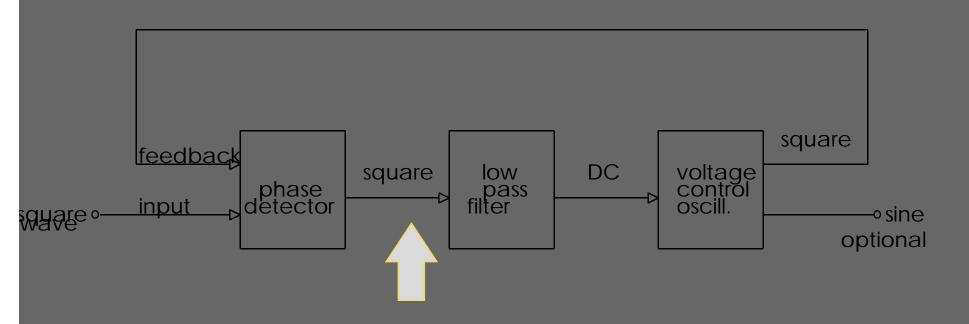


Figure 6-39 page 323







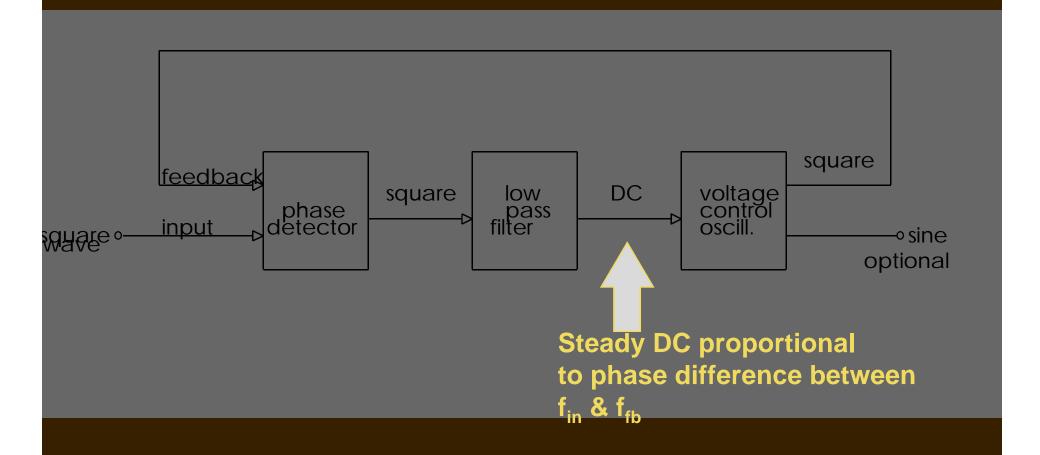


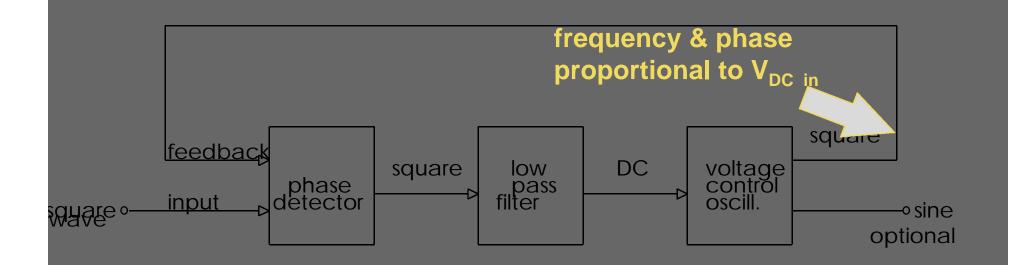
Average value proportional to phase difference between f_{in} and f_{fb} .

Purdue University

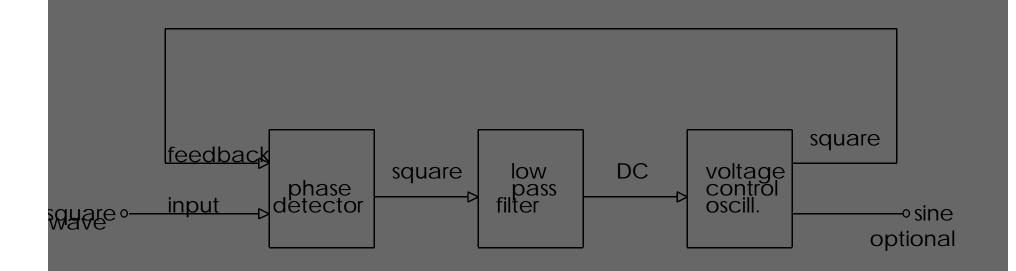
EET 257

Power & RF Electronics





Effects of Variations



Overview

- ◆ Basic Block Diagram
- diagram operation



- ◆ Phase Detector
- ♦ xor CD4046 phase II
- ◆ Loop Filter
- ♦ VCO

Phase Detector

Digital output:

aveage value is proportional to the difference in phase between f_{in} and f_{fb} .

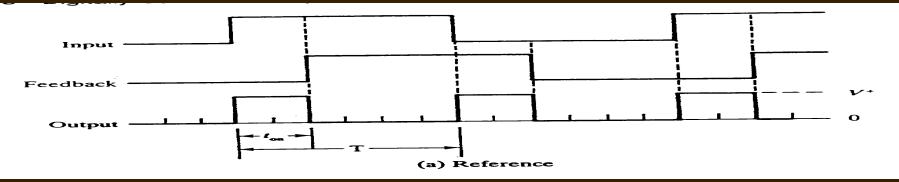
Phase Detector

Digital output:

aveage value is proportional to the difference in phase between f_{in} and f_{fb} .

	Exclusive OR	
input	feedback	output
0	0	0
0	1	1
1	0	1
1	1	0
'	<u> </u>	U

Figure 6-40 a, b, c page 325



Purdue University

EET 257

Power & RF Electronics

Figure 6-40 a, b, c page 325

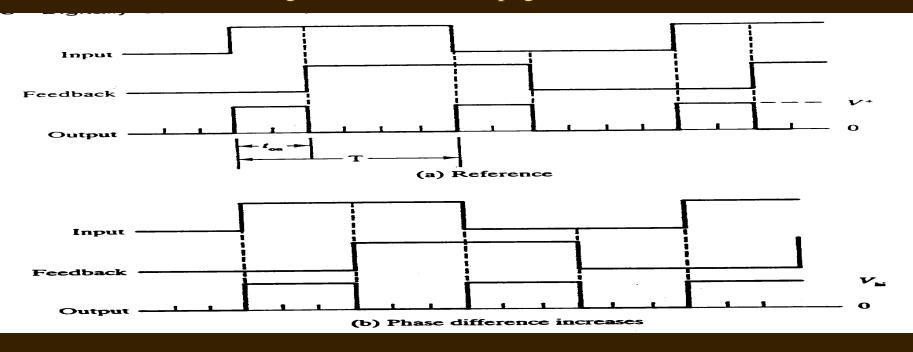
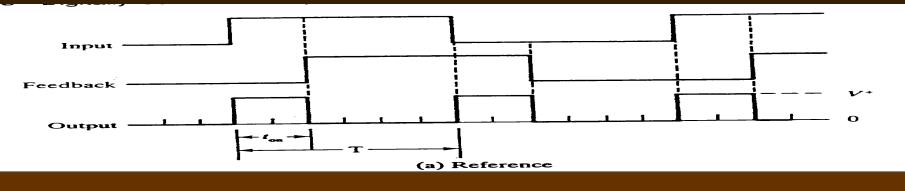


Figure 6-40 a, b, c page 325



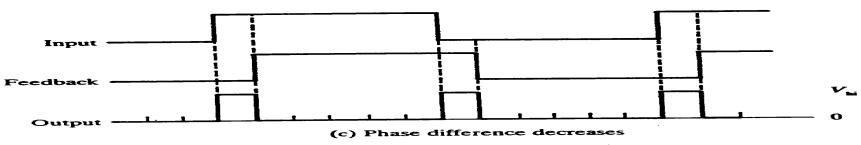


Figure 6-40 Exclusive OR waveforms produce phase detection

Transfer Funtion (Math)

$$V_{AVE} = V_{pk} \frac{t_{on}}{T}$$
 typical pulse width modulation equation

Transfer Funtion (Math)

$$V_{AVE} = V_{pk} \frac{t_{on}}{T}$$
 typical pulse width modulation equation

$$\frac{t_{on}}{T} = \frac{\mathbf{q}}{180^{\circ}}$$

Transfer Funtion (Math)

$$V_{AVE} = V_{pk} \frac{t_{on}}{T}$$
 typical pulse width modulation equation

$$\frac{t_{on}}{T} = \frac{q}{180^{\circ}}$$

$$V_{out\ ave} = V_{hi} \frac{q}{180^{\circ}}$$

output voltage proportional to the difference in phase

Purdue University

EET 257

Power & RF Electronics

What if $f_{in} < or > f_{fb}$?

Figure 6-42 a & b page 328

Figure 6-42 a, b page 327

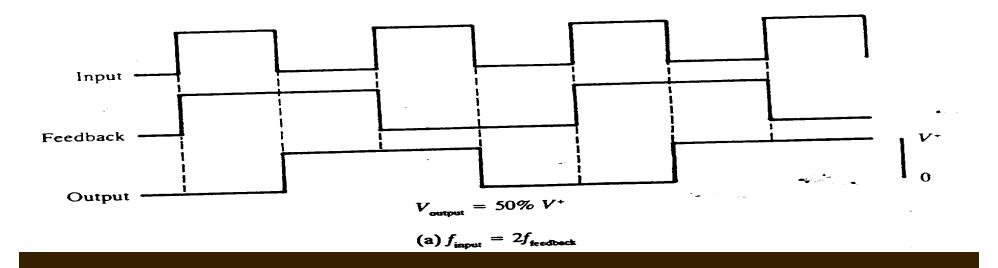
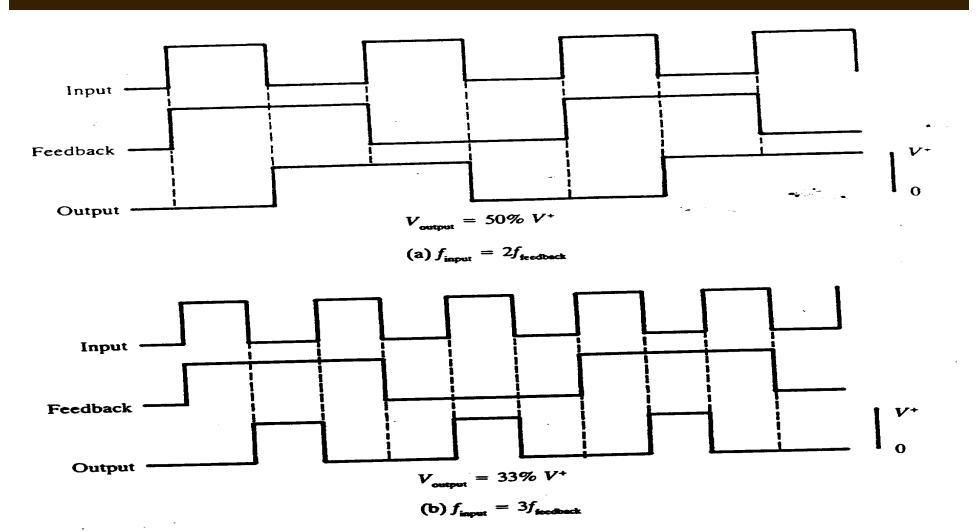


Figure 6-42 a, b page 327



CD4046 phase II detector

CD4046 phase II detector

◆ considerable additional logic

- ◆ considerable additional logic
- \bullet f_{in} > f_{fb} => V_{out} high most of each cycle
 - rest of each cycle V_{out} is open

- ◆ considerable additional logic
- \bullet f_{in} > f_{fb} => V_{out} high most of each cycle
 - rest of each cycle V_{out} is open
- \bullet f_{in} < f_{fb} => V_{out} ground most of each cycle
 - rest of each cycle V_{out} is open

- ◆ considerable additional logic
- \bullet f_{in} > f_{fb} => V_{out} high most of each cycle
 - rest of each cycle V_{out} is open
- \bullet f_{in} < f_{fb} => V_{out} ground most of each cycle
 - rest of each cycle V_{out} is open

- ◆ considerable additional logic
- \bullet f_{in} > f_{fb} => V_{out} high most of each cycle
 - rest of each cycle V_{out} is open
- \bullet f_{in} < f_{fb} => V_{out} ground most of each cycle
 - rest of each cycle V_{out} is open
- \bullet phase of f_{in} leads => v_{out} high while leading
- \bullet phase of f_{in} lags => v_{out} gnd while lagging

Overview

- ◆ Basic Block Diagram
- diagram operation
- ◆ Phase Detector
- ◆ xor CD4046 phase II



- ◆ Loop Filter
- ♦ VCO

♦ digital in; DC out

- ◆ digital in; DC out
- ◆ simple RC is usually OK

- ♦ digital in; DC out
- ◆ simple RC is usually OK
- ◆ slow => very little ripple => stable freq

- ♦ digital in; DC out
- ◆ simple RC is usually OK
- ◆ slow => very little ripple => stable freq
- ◆ slow => sluggish response to changes

- ♦ digital in; DC out
- ◆ simple RC is usually OK
- ◆ slow => very little ripple => stable freq
- ◆ slow => sluggish response to changes
- ♦ fast => quick response to upsets

- ♦ digital in; DC out
- ◆ simple RC is usually OK
- ◆ slow => very little ripple => stable freq
- ◆ slow => sluggish response to changes
- ♦ fast => quick response to upsets
- ◆ fast => ripple on output => variation in freq

Laplace, closed loop analysis:

$$\frac{1}{t s}$$

What size RxC?

Laplace, closed loop analysis:

$$\frac{1}{t s} \qquad \frac{G(s)H(s)}{1+G(s)H(s)}$$

What size RxC?

Laplace, closed loop analysis:

$$\frac{1}{t s} \qquad \frac{G(s)H(s)}{1+G(s)H(s)}$$

Must know transfer function [G(s) & H(s)] of phasell detector and VCO

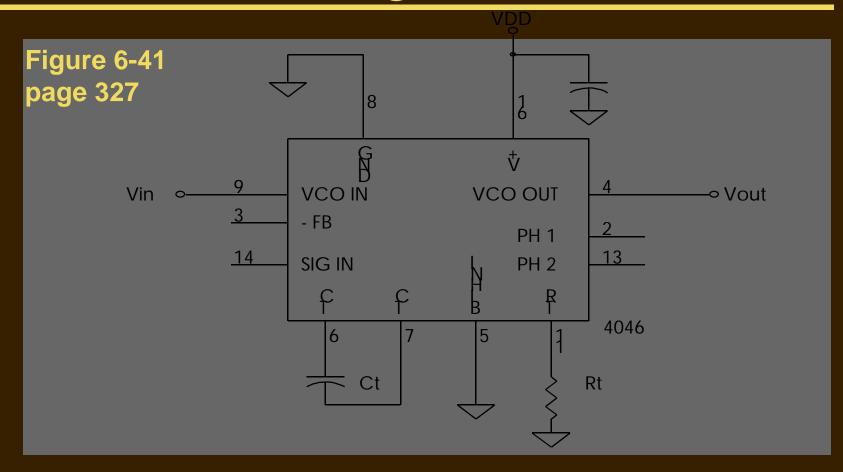
Simplier: Heavily overdamped

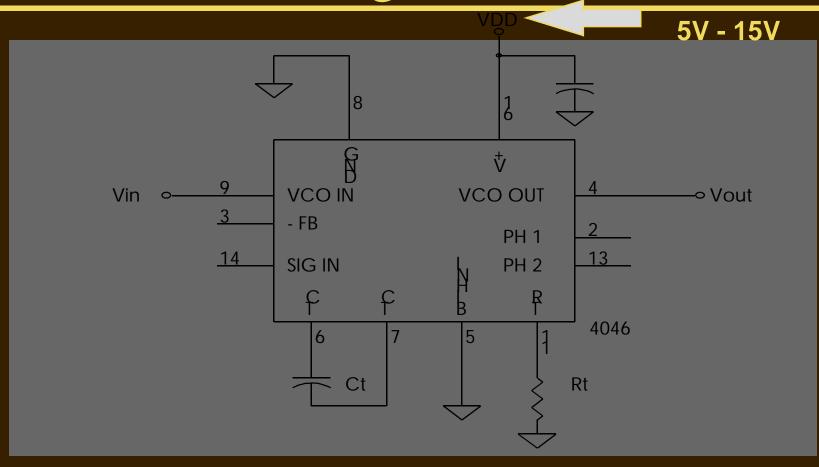
$$t = RC \approx \frac{50\% T_{longest}}{\% ripple}$$

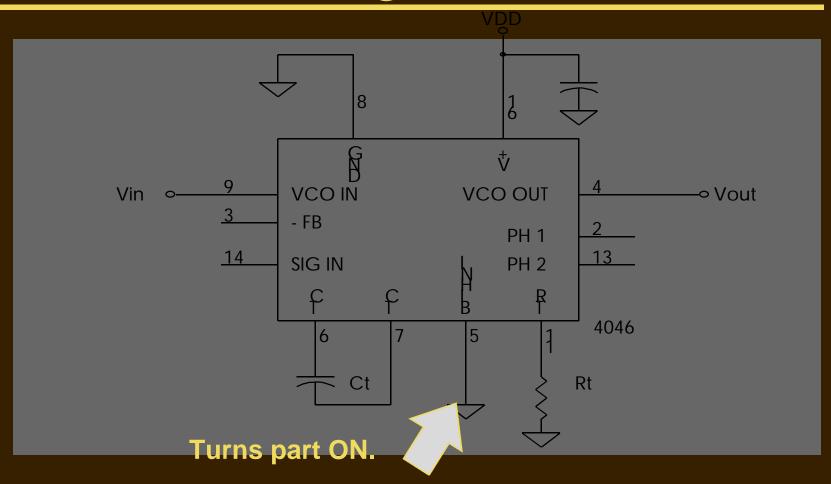
Overview

- ◆ Basic Block Diagram
- diagram operation
- ◆ Phase Detector
- ◆ xor CD4046 phase II
- ◆ Loop Filter





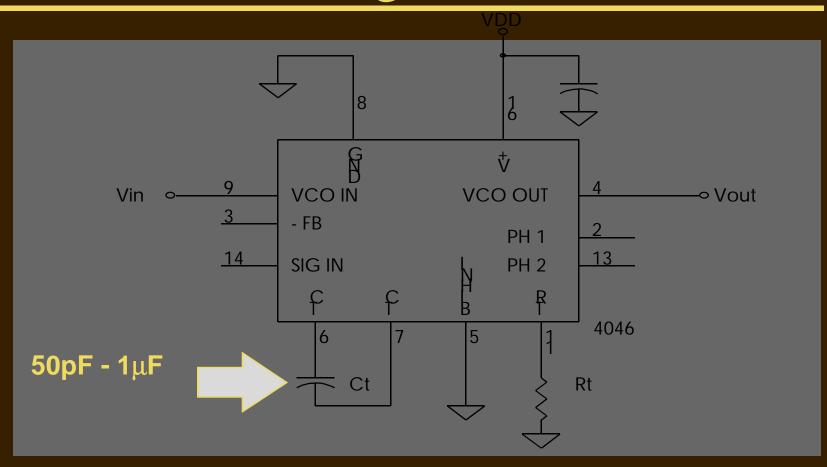


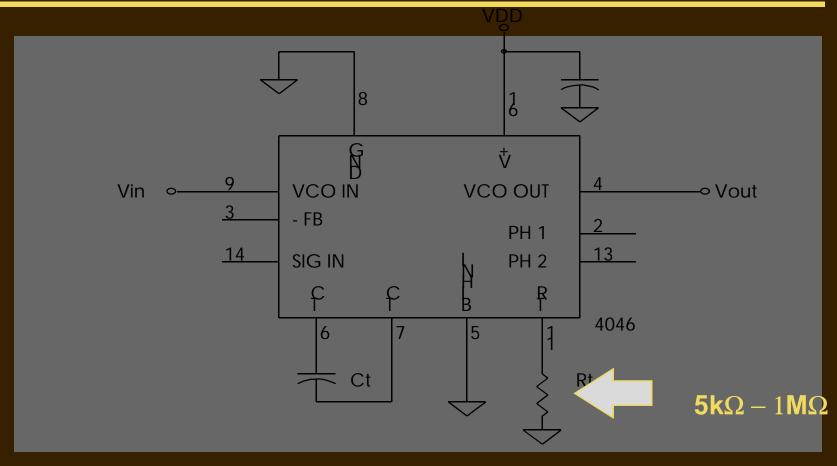


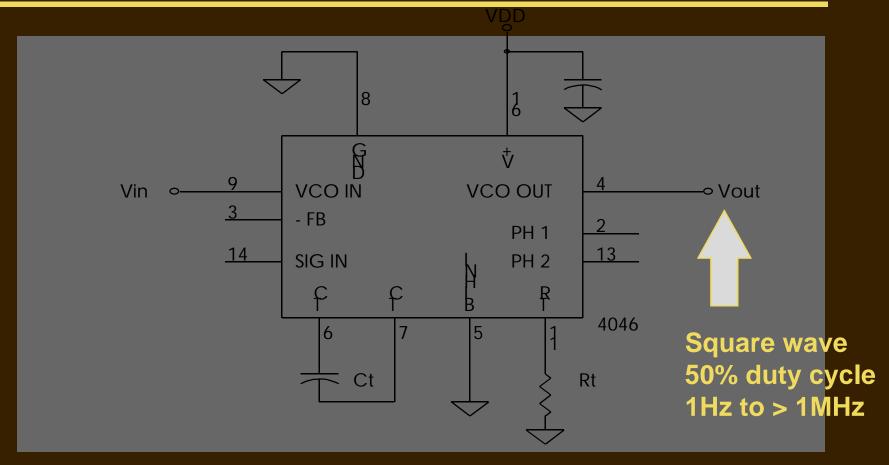
Purdue University

EET 257

Power & RF Electronics







Overview

- ◆ Basic Block Diagram
- diagram operation
- ◆ Phase Detector
- ♦ xor CD4046 phase II
- ◆ Loop Filter
- ♦ VCO