élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2210C/11C/EL2310C/11C/EL2410C/11C

Low Cost, Dual, Triple and Quad Video Op Amps

Features

- Stable at gain of 2 and 100 MHz gain—bandwidth product (EL2211, EL2311, EL2411)
- Stable at gain of 1 and 50 MHz gain—bandwidth product (EL2210, EL2310, EL2410)
- 130V/μs slew rate
- Drives 150Ω load to video levels
- Inputs and outputs operate at negative supply rail
- ±5V or +10V supplies
- −60 dB isolation at 4.2 MHz

Applications

- Consumer video amplifier
- Active filters/integrators
- Cost sensitive applications
- Single supply amplifiers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2210CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2211CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2210CS	−40°C to +85°C	8-lead SO	MDP0027
EL2211CS	−40°C to +85°C	8-lead SO	MDP0027
EL2310CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2311CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2310CS	−40°C to +85°C	14-lead SO	MDP0027
EL2311CS	−40°C to +85°C	14-lead SO	MDP0027
EL2410CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2411CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2410CS	−40°C to +85°C	14-lead SO	MDP0027
EL2411CS	−40°C to +85°C	14-lead SO	MDP0027

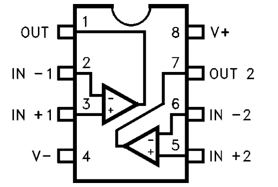
General Description

This family of dual, triple and quad operational amplifiers built using Elantec's Complementary Bipolar process offers unprecedented high frequency performance at a very low cost. They are suitable for any application such as consumer video, where traditional DC performance specifications are of secondary importance to the high frequency specifications. On ±5V supplies at a gain of +1 the EL2210C, EL2310C and the EL2410C will drive a 150Ω load to +2V, −1V with a bandwidth of 50 MHz and a channel to channel isolation of 60 dB or more. At a gain of +2 the EL2211C, EL2311C and EL2411C will drive a 150Ω load to +2V, −1V with a bandwidth of 100 MHz with the same channel to channel isolation. All four achieve 0.1 dB BW at 5 MHz.

The power supply operating range is fixed at ±5V or +10/0V. In single supply operation the inputs and outputs will operate to ground. Each amplifier draws only 7 mA of supply current.

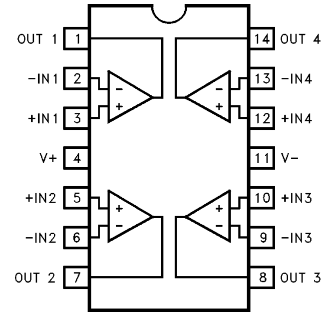
Connection Diagrams

EL2210C/EL2211C



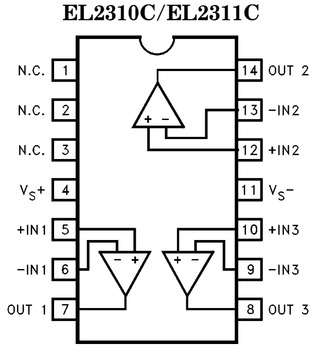
2210–1

EL2410C/EL2411C



2210–2

EL2310C/EL2311C



2210–5

Absolute Maximum Ratings

Total Voltage Supply	18V	Power Dissapation	See Curves
Input Voltage	±Vs	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	6V	Operating Temperature Range	−40°C to +85°C
Peak Output Current	75 mA per amplifier		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

EL2210, EL2310, EL2410

DC Electrical Characteristics V_S = ±5V, R_L = 1 KΩ, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			10	20	I	mV
		EL2310C only		10	25	I	mV
		EL2311C only		5	25	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	μV/°C
I_B	Input Bias Current		−15	−7	−3	I	μA
I_{OS}	Input Offset Current			0.5	1.5	I	μA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	V_{OUT} = ±2V, R_L = 1 KΩ	160	250		I	V/V
		V_{OUT} = +2V/0V, R_L = 150Ω	160	250		V	
PSRR	Power Supply Rejection	V_S = ±4.5V to ±5.5V	50	60		I	dB
CMRR	Common Mode Rejection	V_{CM} = ±2.4V, V_{OUT} = 0V	60	80		I	dB
CMIR	Common Mode Input Range	V_S = ±5V		−5/+3		V	V
V_{OUT}	OutputVoltage Swing	R_L = R_F = 1 KΩ R_L to Gnd	−2.5	−3, 3	2.7	I	V
		R_L = R_F = 1 KΩ +150Ω to Gnd	−0.45	−0.6, 2.9	2.5	I	
		R_L = R_F = 1 KΩ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load (per channel)	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		±6.5	V	V
		Single Supply	9		13	V	

TD is 4.0in

EL2211, EL2311, EL2411

DC Electrical Characteristics $V_S = \pm 5V$, $R_L = 1\ K\Omega$, $A_V = +2$, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			5	12	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	μV/°C
I_B	Input Bias Current		−15	−7	−3	I	μA
I_{OS}	Input Offset Current			0.5	1.5	I	μA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	$V_{OUT} = \pm 2V$, $R_L = 1\ K\Omega$	250	380		I	V/V
		$V_{OUT} = +2V/0V$, $R_L = 150\Omega$	250	380		V	
PSRR	Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 5.5V$	55	68		I	dB
CMRR	Common Mode Rejection	$V_{CM} = \pm 2.5V$, $V_{OUT} = 0V$	70	90		I	dB
CMIR	Common Mode Input Range	$V_S = \pm 5V$		−5/+3		V	V
V_{OUT}	Output Voltage Swing	$R_L = R_F = 1\ K\Omega$ R_L to Gnd	2.5	−3.5, 3.3	2.7	I	V
		$R_L = R_F = 1\ K\Omega + 150\Omega$ to Gnd	−0.45	−0.6, 2.9	2.5	I	
		$R_L = R_F = 1\ K\Omega$ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		±6.5	V	V
		Single Supply	9		13	V	

TD is 4.3in

EL2210, EL2310, EL2410

Closed-Loop AC Characteristics $V_S = \pm 5V$, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min.	Typ.	Max.	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$A_V = +1$		110		V	MHz
BW	±0.1 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$A_V = +1$		12		V	MHz
GBWP	Gain Bandwidth Product			55		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		85	130		V	V/μs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2		V	ns
OS	Overshoot	0.1V Step		15		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% ($A_V = 1$)	$V_S = \pm 5V$, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.1		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.2		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from T_{MIN} to T_{MAX}
Note 3: For $V_S = \pm 5V$, $V_{OUT} = 4\ V_{PP}$. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})
Note 4: Video performance measured at $V_S = \pm 5V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$.

TD is 3.1in

EL2211, EL2311, EL2411

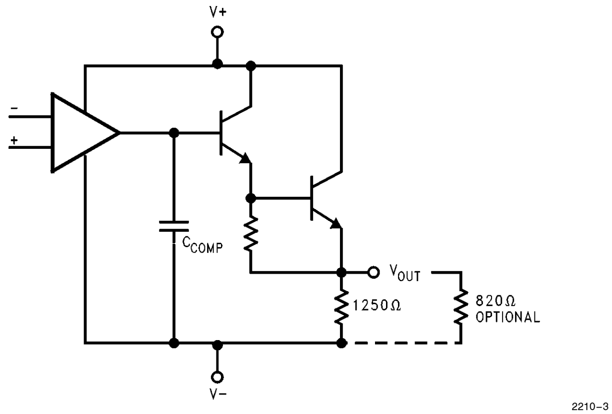
Closed-Loop AC Characteristics $V_S = \pm 5V$, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +2		100		V	MHz
BW	±0.1 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +2		8		V	MHz
GBWP	Gain Bandwidth Product			130		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		100	140		V	V/μs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2.5		V	ns
OS	Overshoot	0.1V Step		6		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% (A_V = 1)	V_S = ±5V, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.04		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.15		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

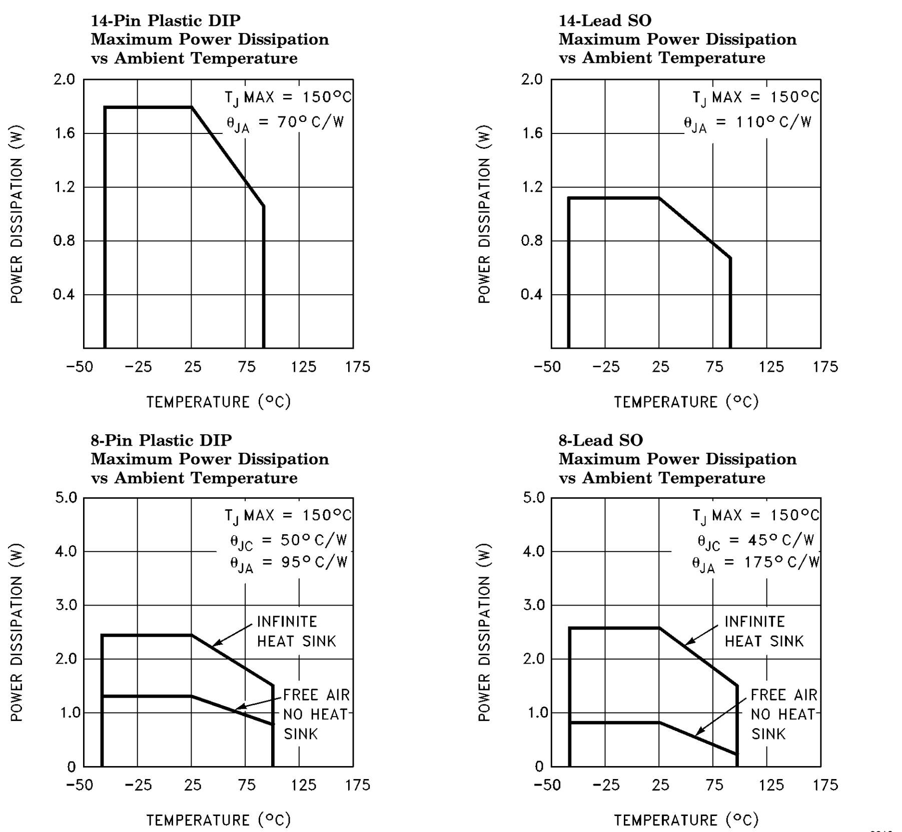
Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from T_{MIN} to T_{MAX}
Note 3: For V_S = ±5V, V_{OUT} = 4 V_{PP}. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})
Note 4: Video performance measured at V_S = ±5V, A_V = +2 with 2 times normal video level across R_L = 150Ω.

TD is 3.1in

Simplified Block Diagram



Typical Performance Curves



Application Information

Product Description

The EL2210, EL2310 and EL2410 are dual, triple and quad operational amplifiers stable at a gain of 1. The EL2211, EL2311 and the EL2411 are dual, triple and quad operational amplifiers stable at a gain of 2. All six are built on Elantec's proprietary complimentary process and share the same voltage mode feedback topology. This topology allows them to be used in a variety of applications where current mode feedback amplifiers are not appropriate because of restrictions placed on the feedback elements. These products are especially designed for applications where high bandwidth and good video performance characteristics are desired but the higher cost of more flexible and sophisticated products are prohibitive.

Power Supplies

These amplifiers are designed to work at a supply voltage difference of 10V to 12V. These amplifers will work on any combination of ± supplies. All Electrical characteristics are measured with ±5V supplies. Below 9V total supply voltage the amplifiers' performance will degrade dramatically. The quiescent current is a direct function of total supply voltage. With a total supply voltage of 12V the quiescent supply current will increase from a typical 6.8 mA per amplifier to 8.5 mA per amplifer.

Output Swing vs Load

Please refer to the simplified block diagram. These amplifiers provide an NPN pull-up transistor output and a passive 1250Ω pull-down resistor to the most negative supply. In an application where the load is connected to V_S- the output voltage can swing to within 200 mV of V_S-. In split supply applications where the DC load is connected to ground the negative swing is limited by the voltage divider formed by the load, the internal 1250Ω resistor and any external pull-down resistor. If R_L were 150Ω then it and the 1250Ω internal resistor limit the maximum negative swing to (V_{EE}(150/1250+150)) or −0.53V. The negative swing can be increased by adding an external resistor of appropriate value from the output to the negative supply. The simplified block diagram shows an 820Ω external pull-down resistor. This resistor is in parallel with the internal 1250Ω resistor. This will increase the negative swing to V_{EE} (150/((1250 * 820/(1250 + 820) + 150) or −1.16V.

Power Dissipation and Loading

Without any load and a 10V supply difference the power dissipation is 70 mW per amplifier. At 12V supply difference this increases to 105 mW per amplifier. At 12V this translates to a junction temperature rise above ambient of 33° for the dual and 40° for the quad amplifier. When the amplifiers provide load current the power dissipation can rapidly rise.

In ±5V operation each output can drive a grounded 150Ω load to more than 2V. This operating condition will not exceed the maximum junction temperature limit as long as the ambient temperature is below 85°C, the device is soldered in place, and the extra pull-down resistor is 820Ω or more.

If the load is connected to the most negative voltage (ground in single supply operation) you can easily exceed the absolute maximum die temperature. For example the maximum die temperature should be 150°C. At a maximum expected ambient temperature of 85°C, the total allowable power dissipation for the SO-8 package would be:

P_D = (150 − 75)/180°C/W = 416 mW

At 12V total supply voltage each amplifier draws a maximum of 8.5 mA and dissipates 12V * 8.5 mA = 100 mW or 200 mW for the dual amplifier. Which leaves 216 mW of increased power due to the load. If the load were 150Ω connected to the most negative voltage and the maximum voltage out were V_S- +2V the load current would be 13 mA. Then an extra 266 mW ((12V − 2V) * 13.3 mA * 2) would be dissipated in the EL2210 or EL2211. The total dual amplifier power dissipation would be 266 mW + 200 mW = 466 mW, more than the maximum 416 mW allowed. If the total supply difference were reduced to 10V, the same calculations would yield 170 mW quiescent power dissipation and 213 mW due to loading. This results in a die temperature of 143°C (75°C + 69°C).

Application Information — Contd.

In the above example, if the supplies were split ±6V and the 150Ω loads were connected to ground, the load induced power dissipation would drop to 106 mW (13.3 mA * (6 − 2) * 2) and the die temperature would be below the rated maximum.

Video Performance

Following industry standard practices (see EL2044 applications section) these six devices exhibit good differential gain (dG) and good differential phase (dP) with ±5V supplies and an external 820Ω resistor to the negative supply, in a gain of 2 configuration. Driving 75Ω back terminated cables to standard video levels (1.428V at the amplifier) the EL2210, EL2310 and EL2410 have dG of 0.1% and dP of 0.2°. The EL2211, EL2311 and the EL2411 have dG of 0.04% and dP of 0.15°.

Due to the negative swing limitations described above, inverted video at a gain of 2 is just not practical. If swings below ground are required then changing the extra 820Ω resistor to 500Ω will allow reasonable dG and dP to approximately −0.75 mV. The EL2211, EL2311 and EL2411 will achieve approximately 0.1%/0.4° between 0V and −0.75V. Beyond −0.75V dG and dP get worse by orders of magnitude.

Differential gain and differential phase are fairly constant for all loads above 150Ω. Differential phase performance will improve by a factor of 3 if the supply voltage is increased to ±6V.

Output Drive Capability

None of these devices have short circuit protection. Each output is capable of more than 100 mA into a shorted output. Care must be used in the design to limit the output current with a series resistor.

Printed-Circuit Layout

The EL2210C/EL2211C/EL2310C/EL2311C/EL2410C/EL2411C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 KΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wirewound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

January 1996 Rev D

EL2210/EL2310/EL2410 Macromodel

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* Revision A, June 1994
* Application Hints:
*
* A pull down resistor between the output and V− is recommended
* to allow output voltages to swing close to V−. See datasheet
* for recommended values.
*
* Connections:        +In
*                     |      −In
*                     |      |      V+
*                     |      |      |      V−
*                     |      |      |      |      Vout
*                     |      |      |             |
.subckt EL2210/EL     3      2      8      4      1
q1 20 3 24 qp
q2 21 2 25 qp
q3 10 10 26 qp
q4 12 10 11 qp
q5 14 10 13 qp
q6 19 19 20 qn
q7 14 19 21 qn
q8 8 14 15 qn
q9 8 16 17 qn 10
r1 24 12 350
r2 12 25 350
r3 8 26 250
r4 8 11 150
r5 8 13 240
r6 20 4 150
r7 21 4 150
r8 15 17 700
r9 1 4 1250
r10 15 16 40
r11 17 1 15
r12 10 19 10K
r13 14 22 20
c1 22 4 0.45pF
c2 22 19 1pF
d1 1 14 dcap
.model qn npn(bf=150 tf=0.05nS)
.model qp pnp(bf=90 tf=0.05nS)
.model dcap d(rs=200 cjo=le- 12 vj=0.8 tt=100e-9)
.ends
```

EL2211/EL2311/EL2411 Macromodel

```
* Revision A, June 1994
* Application Hints:
*
* A pull down resistor between the output and V− is recommended
* to allow output voltages to swing close to V−. See datasheet
* for recommended values.
*
* Connections:    +In
*                  |   −In
*                  |     |   V+
*                  |     |   |  V−
*                  |     |   |  |  Vout
*                  |     |   |  |   |
.subckt EL2211/EL  3     2   8  4   1
q1 20 3 24 qp
q2 21 2 25 qp
q3 10 10 26 qp
q4 12 10 11 qp
q5 14 10 13 qp
q6 19 19 20 qn
q7 14 19 21 qn
q8 8 14 15 qn
q9 8 16 17 qn 10
r1 24 12 175
r2 12 25 175
r3 8 26 250
r4 8 11 150
r5 8 13 240
r6 20 4 150
r7 21 4 150
r8 15 17 700
r9 1 4 1250
r10 15 16 40
r11 17 1 15
r12 10 19 10K
r13 14 22 20
c1 22 4 0.42pF
c2 22 19 1pF
d1 1 14 dcap
.model qn npn(bf=150 tf=0.05nS)
.model qp pnp(bf=90 tf=0.05nS)
.model dcap d(rs=200 cjo=le- 12 vj=0.8 tt=100e-9)
.ends
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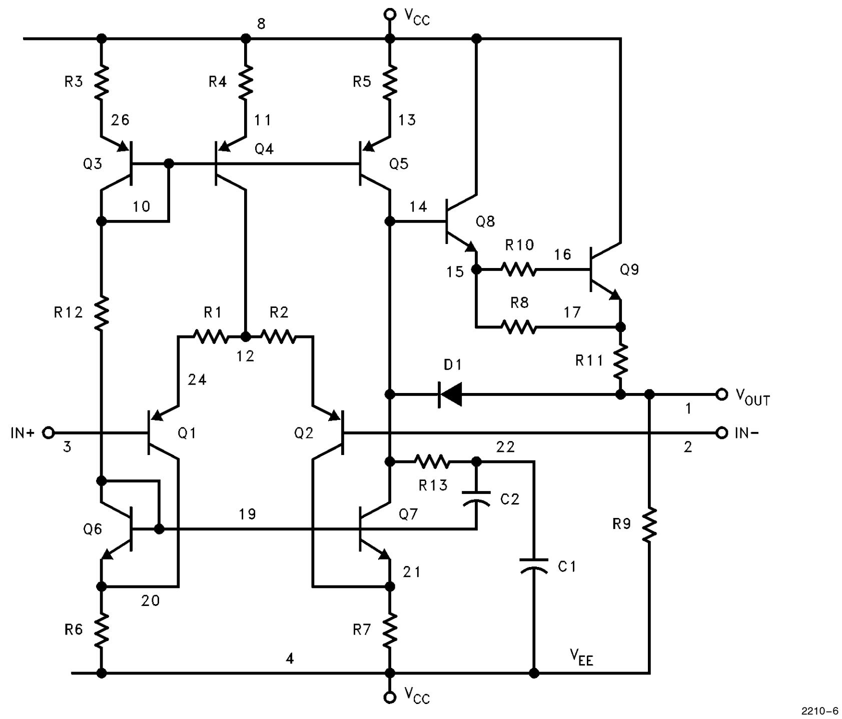
TD is 5.7in


VCC
8
R3
R4
R5
26
11
13
Q3
Q4
Q5
10
14
Q8
R10
16
15
Q9
R12
R1
R2
R8
17
12
R11
D1
24
VOUT
1
IN+
3
Q1
Q2
IN-
2
22
R13
C2
19
Q7
Q6
R9
21
C1
20
R6
R7
4
VEE
VCC
2210-6

EL2210C/11C/EL2310C/11C/EL2410C/11C
Low Cost, Dual, Triple and Quad Video Op Amps

General Disclaimer
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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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January 1996 Rev D

Printed in U.S.A.