AN1491
APPLICATION NOTE

IGBT BASICS

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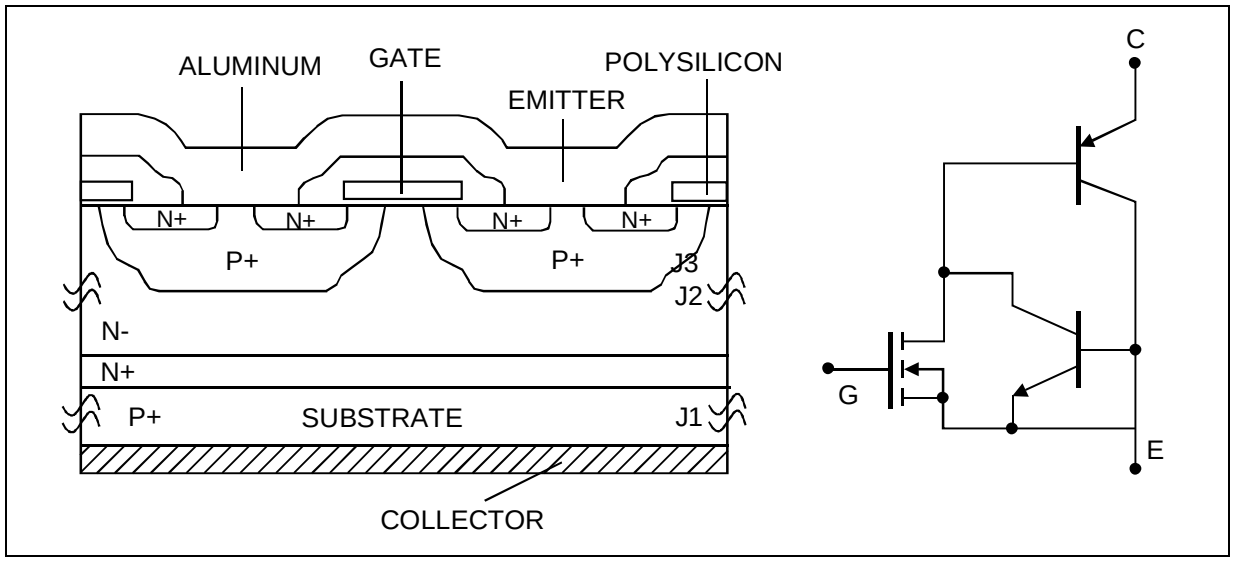
1. INTRODUCTION.

IGBTs (Insulated Gate Bipolar Transistors) combine the simplicity of drive and the excellent fast switching capability of the MOSFET structure with the ability to handle high current values typical of a bipolar device. IGBTs also offer good behavior in terms of voltage drop. IGBT technology, developed in the early 1980s, has quickly gained market share for applications exceeding 400V and that work up to 130kHz. This paper includes a brief description of the structure and the physics of the device, followed by an analysis of the principal static and dynamic characteristics. Further details about the behavior in operation will also be analyzed and discussed in order to give a complete overview of the main parameters, features, and static and dynamic behaviors of this power component.

2. IGBT STRUCTURE AND OPERATION.

Figure 1: IGBT Structure And Equivalent Schematic



IGBTs are a natural evolution of the vertical Power MOSFETs for high current, high voltage applications and fast end-equipment. This device eliminates the main disadvantage of current high voltage power MOSFETs characterized by an high value of $R_{DS(on)}$ caused by the high resistivity of the source-drain path necessary to obtain a high breakdown voltage BV_{DSS}. The power conduction losses at high current levels are considerably less in IGBT technology even when compared with the latest generation of Power MOSFET devices that have been greatly improved in terms of $R_{DS(on)}$. The lower voltage drop,

translated into a low $V_{CE(sat)}$, together with the device's structure allow a higher current density than a standard bipolar device simplifying the IGBTs driver schematic as well. The vertical section depicted in figure 1 together with the equivalent circuit shows IGBTs basic structure.

3. TURN-ON.

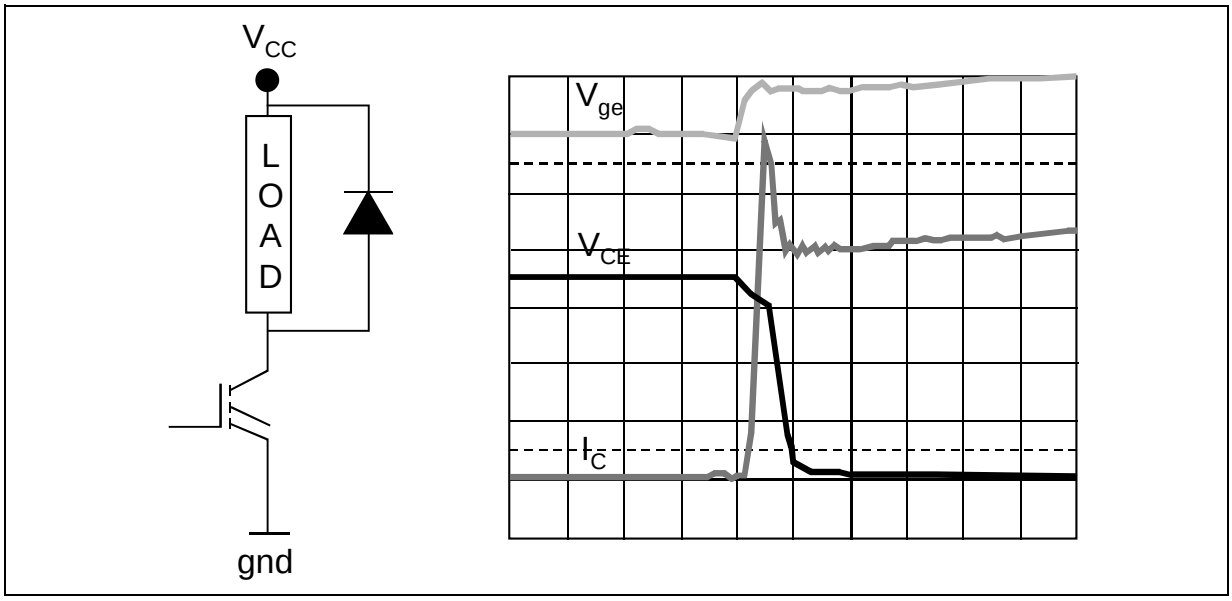
The structure of the silicon die is evidently similar to that of a Power MOSFET with the fundamental difference of the addition of a P+ substrate and an N+ buffer layer (absent in NPT-non-punch-through-IGBT technology). This is represented in the equivalent schematic (figure 1), with a MOSFET driving two bipolar devices. The presence of the substrate creates a junction J1 between the P+ and the N zone of the body.

When the positive gate bias allows the inversion of the P base region under the gate, an N channel is created, with a flow of electrons, generating a current in the exact same way as a Power MOSFET. If the voltage caused by this flux is in the range of 0.7V, then J1 is forward biased and some holes are injected in the N- region, modulating the resistance between anode and cathode, in this way decreasing the overall power conduction losses and a second flow of charges starts.

The final result is the contemporary presence of two different typologies of current inside the semiconductor's layers:
- an electron flux (MOSFET current);
- a hole current (bipolar).

The typical waveforms with an inductive load are reported in figure 2.

Figure 2: Typical Waveforms During Turn-On

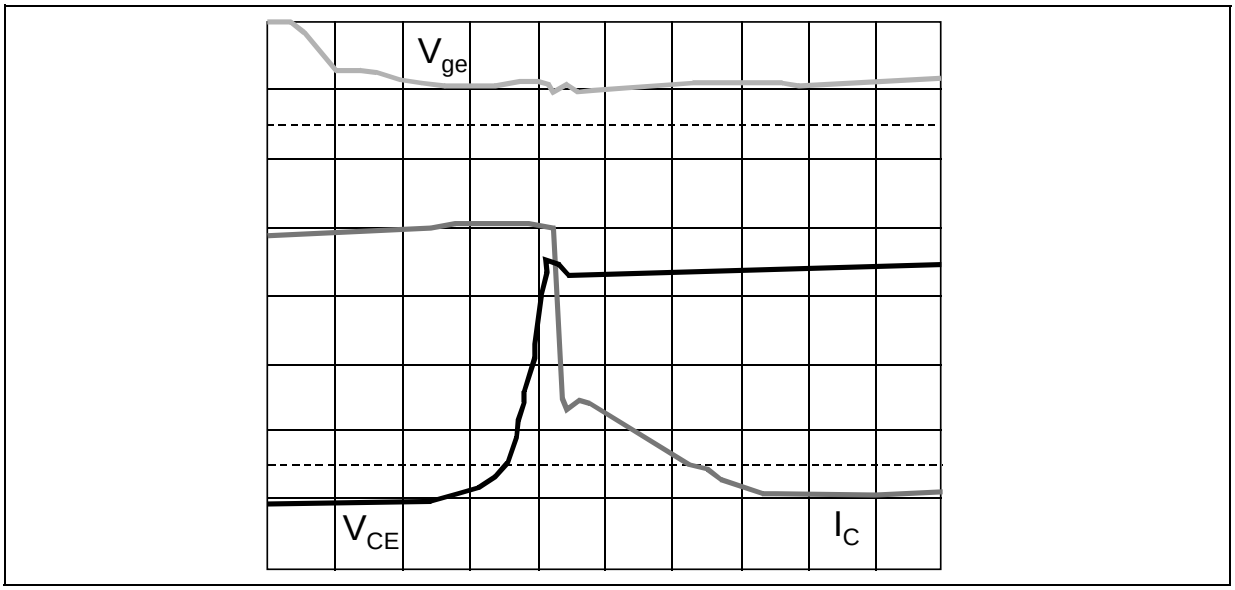


4. TURN-OFF.

When a negative bias is applied to the gate or the gate voltage falls below the threshold value, the channel is inhibited and no holes are injected in the N- region. In any case even if the MOSFET current decreases rapidly in the switching off phase, the collector current gradually reduces because there are minority carriers still present in the N layer, immediately after the start of commutation. The decrease in value of this residual current (tail) is strictly dependent on the density of these charges in turn-off that is linked to several factors as the amount of dopant, dopant typology, layers' thickness and temperature.

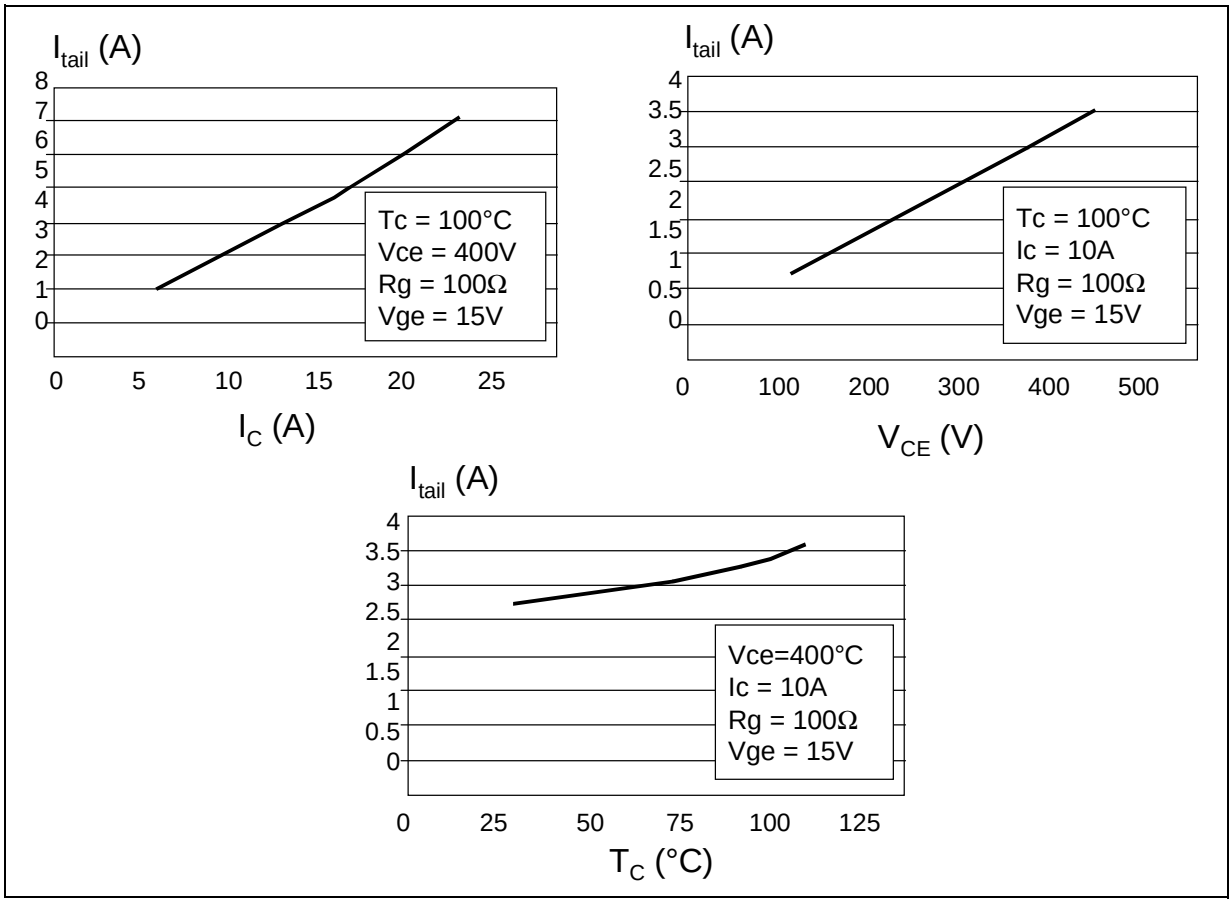
The minority carrier's density decay gives the characteristic tail shape (reported in figure 3) to the collector current that is responsible for:
- an increase in power losses;
- cross conduction problems, in peculiar appliances where the free-wheeling diodes are used.

Figure 3: Typical Waveforms During Turn-Off



Considering that the tail current is linked to the minority carrier's recombination its value and shape are strictly related to the holes' mobility strictly related to the temperature reached by the die, I_C and V_{CE}. So depending on the temperature reached, it is possible to reduce the undesirable effect of this current acting on the end equipment design, as indicated in the graphs below, where the tail current (I_{tail}) behavior related to V_{CE}, I_C, and T_C is depicted (figure 4).

Figure 4: I_{tail} Dependance From I_C, T_C, and V_{CE}



5. REVERSE BLOCKING.

When a negative voltage is applied to the collector then J1 is reverse biased and the depletion layer expands to the N- region. This mechanism is fundamental because an excessive reduction of this layer's thickness does not obtain a valid blocking capability. On the other hand increasing the dimension of this region too much consistently elevates the voltage drop.

This second option explains clearly why NPT devices have a higher voltage drop when compared with an equivalent (equal I_C and speed) PT part.

6. FORWARD BLOCKING.

When gate and emitter are shorted and a positive voltage is applied to the collector terminal the P/N- the J3 junction is reverse biased. Again it is the depletion layer in the N- drift region that withstands the voltage applied.

7. LATCH UP.

IGBTs contains a parasitic PNPN thyristor between the collector and the emitter, as evidenced in figure 1. Under particular conditions this parasitic device enters in turn on. This causes an increase in the current flowing between emitter and collector, a lose of control of the equivalent MOSFET and generally the disruption of the component. The turn-on of the thyristor is known as latch up of the IGBT, more in detail

the causes of this failure are different and strictly dependent on the status of the device.

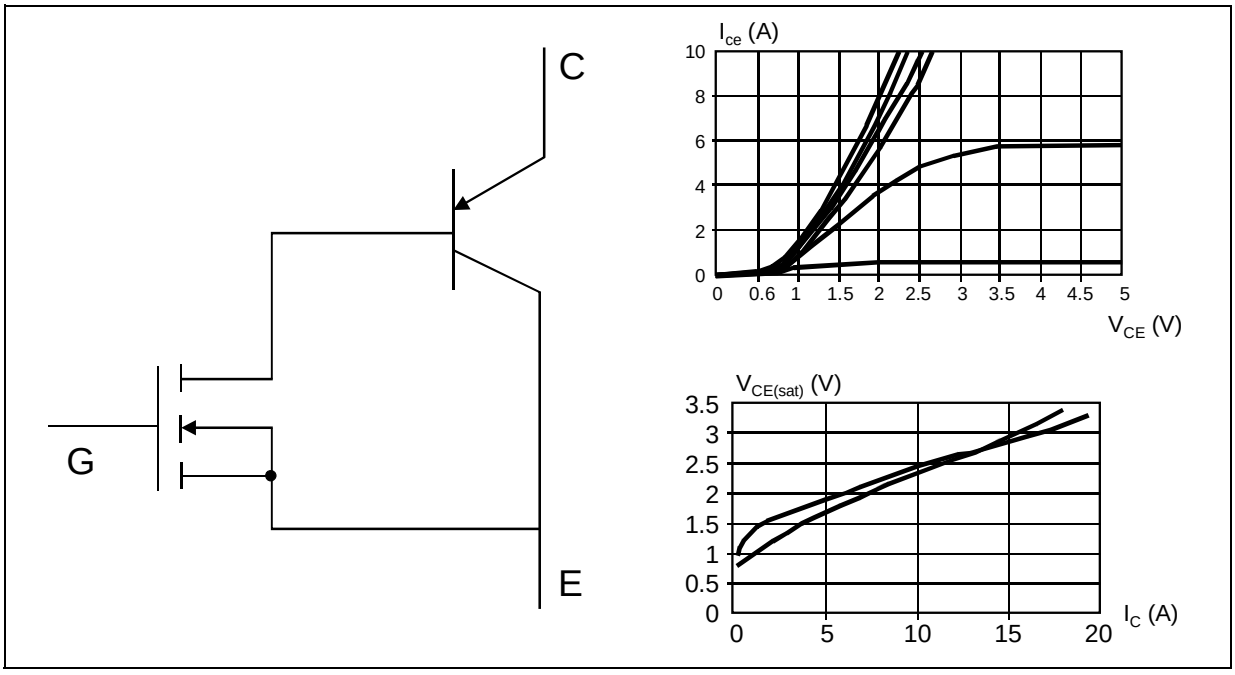
In general a static and a dynamic latch up are distinguished by the following:
- Static latch up happens when the device is in full conduction.
- Dynamic latch up takes place only during turn-off. This peculiar phenomenon strongly limits the safe operating area.

In order to avoid this dangerous effect of the parasitic NPN and PNP transistors it is necessary:
- to prevent the turn-on of the NPN part, modifying both the layout and doping level;
- to reduce the overall current gain of the NPN and PNP transistors.

Furthermore the latching current is strictly dependent on the junctions' temperature since it affects the current gains of PNP and NPN parts; moreover with an increase of temperature, together with the gains, the resistance of the P base region becomes higher, aggravating the overall behavior. So particular attention must be paid by the manufacturer of the parts in order keep distant the maximum collector current value to the one of the latching current. In general the ratio is in the order of 1 to 5.

8. FORWARD CONDUCTION CHARACTERISTICS.

Figure 5: Forward Characteristics And Equivalent Schematic Operation



The IGBT in conduction can be modeled, as a first approximation, as a PNP transistor driven by a Power MOSFET. Figure 5 only shows the elements of the structure necessary for the understanding of physic the device in operation (parasitic elements are not considered).

As showed in the graph reporting I_C as a function of V_{CE} (static characteristic), the collector current I_C does not flow if the voltage drop between anode and cathode does not exceed 0.7V even if the gate signal allows the formation of the MOSFET channel, as evidenced in the graphs.

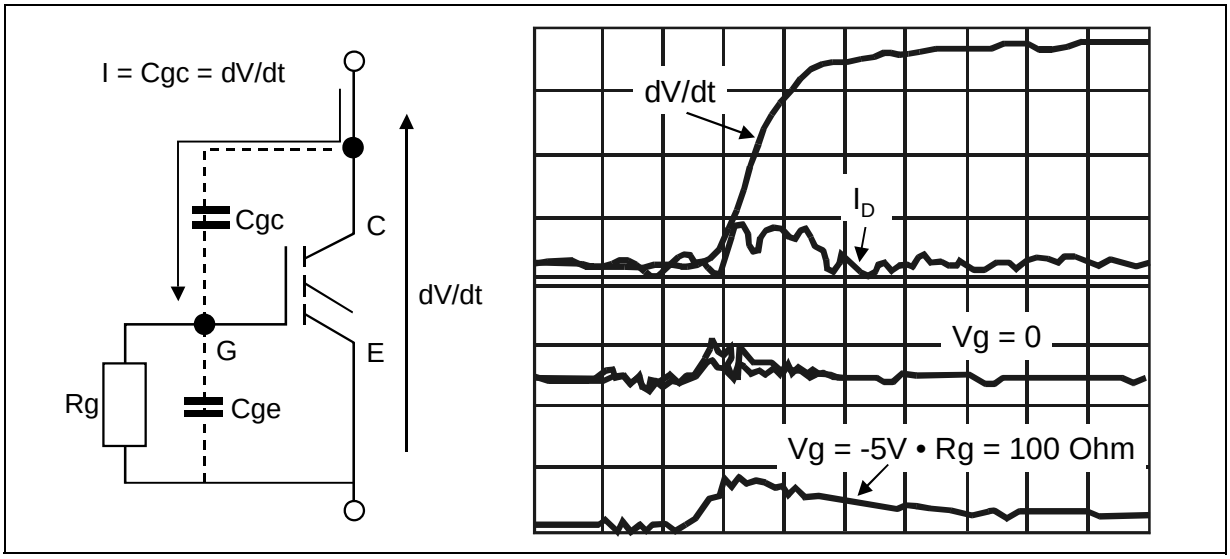
When the voltage across the channel is greater than V_{GE}-V_{th} the current is saturated and the output resistance becomes infinite. As the IGBT structure includes both a bipolar and a Power MOSFET, its temperature characteristics depend on the net effect of the two components that have contrasting properties. The Power MOSFET has a positive temperature coefficient, while the bipolar's temperature coefficient is negative. The figure shows the change in $V_{CE(sat)}$ as a function of the collector current for two different values of junction temperature. This aspect becomes crucial when it is necessary to parallel two or more devices and can only be solved by selecting a device to be paralleled, based on $V_{CE(sat)}$ at a certain current rate. Sometimes the use of a NPT device for an easy parallel is helpful, but the payback is an increase of voltage drop when compared with a PT part with the same current level and speed.

9. DYNAMIC CHARACTERISTICS.

The dynamic characteristics indicate the behavior of the device during the switching phases. Considering the equivalent circuit of the IGBT, it is evident that in order to control the device the MOSFET part must be driven.

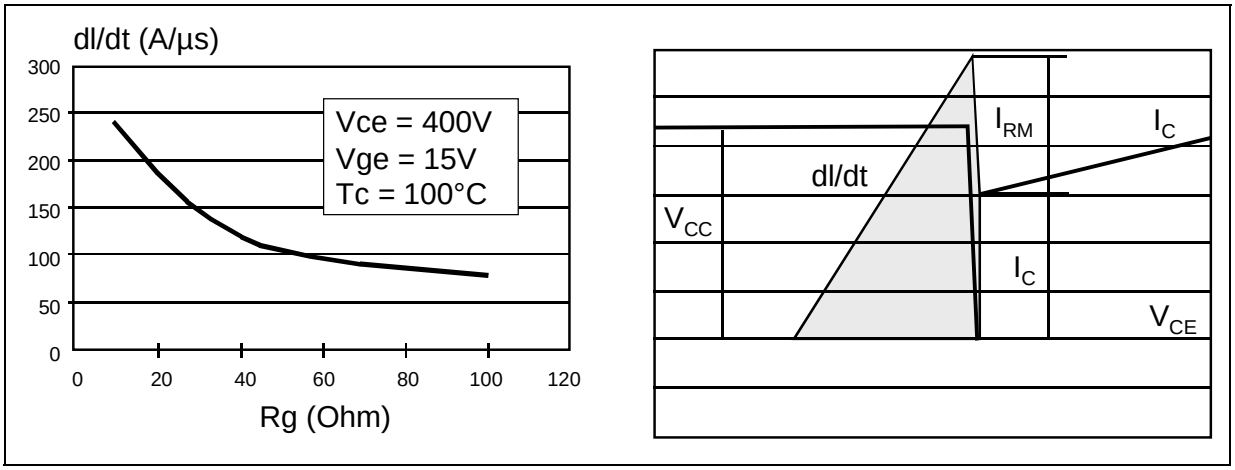
This means the driver system is practically the same as the MOSFET's one and less complex than the bipolar's driver system. As explained before when the positive gate bias is provided via gate, an N channel is created in the MOSFET part. If the voltage caused by this flux is in the range of 0.7V the P+/ N- junction is forward biased and the minority carriers are injected in the N- region, creating a hole bipolar current. The turn-on time is a function of the output impedance of the drive circuit and the applied gate voltage. It is possible to control the speed of the device by varying the value of the gate resistance Rg (figure 6), obtaining in this way a different charge velocity of the input parasitic capacitances Cge, Cgc.

Figure 6: Rg Effect On dV/dt



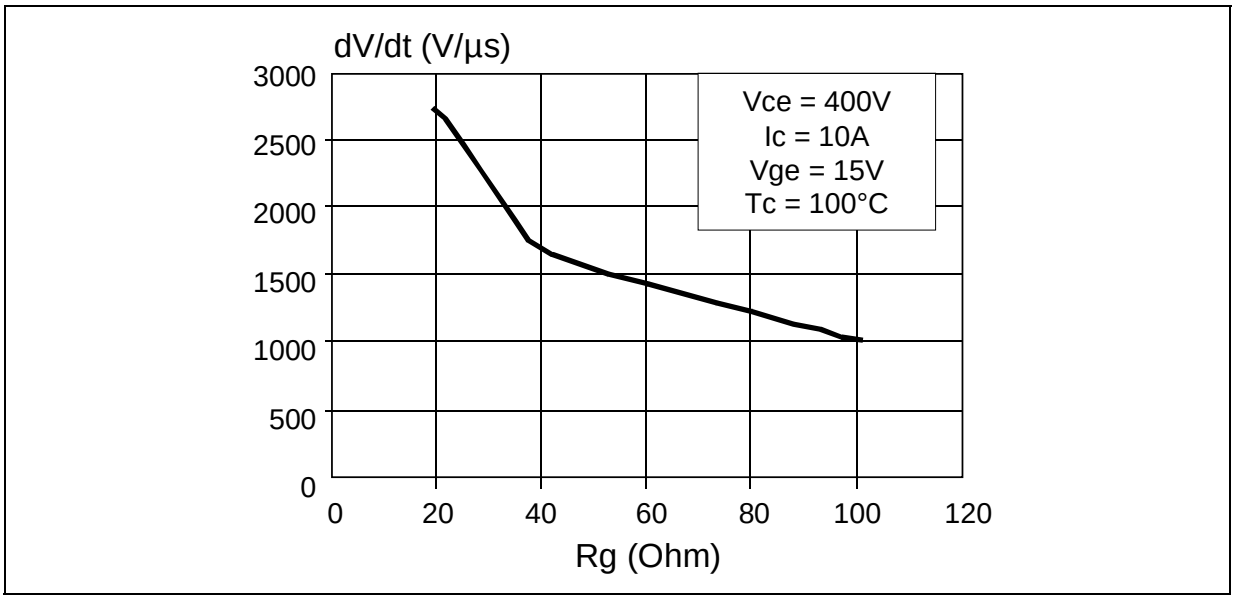
In other words, by varying the Rg is it possible to vary the time constant of the parasitic net (reported in figure) equal to Rg (Cge+Cgc) and then dv/dt. The gate drive voltage generally adopted and reported in the datasheets is 15V. In figure 7 waveforms for the switching of an inductive load are reported, while di/ dt as a function of Rg is showed in figure 8, where the effect of gate resistance on the turn on velocity of the IGBTs is evident.

Figure 7: Rg Effect On dI/dt And Energy In Turn-On



Therefore, the Rg value strongly impacts the power losses, since its variation also affects the dv/dt slopes, as shown in figure 8.

Figure 8: dV/dt Dependance On Rg

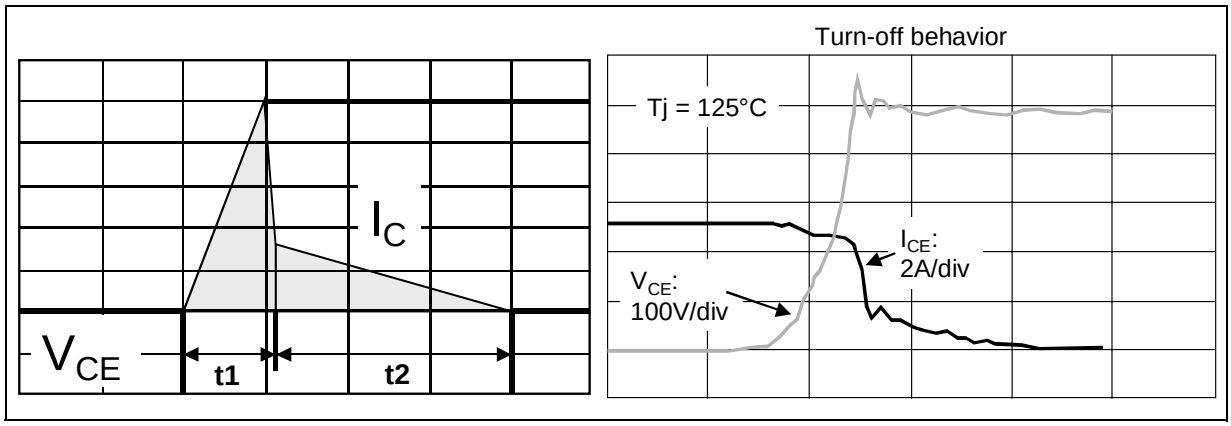


During turn-off the behavior discussed in the equivalent model with a dual characteristic of both power MOSFET and BJT devices reemerges again. When the signal to the gate decreases to a value at which the Miller effect begins, V_{CE} starts to increase. As explained before after V_{CE} reaches its maximum level, dependent on the driver and affected also by the Cge together with Cgcmiller, the current does not immediately go to zero but assumes the typical shape of a tail, whose length is strictly dependent on the life times of the minority carriers.

These charges have been injected into the N- region during the positive bias of the device and it is the main responsible for the worst behavior of IGBTs against MOSFETs in switching. There are several ways to reduce this effect. For example it is possible to reduce the percentage of the holes injected in turn-on

from P+ substrate and in parallel to increase the recombination-speed, by an increase in the dopant level and the thickness of the buffer layer. The withdrawal is a reduction in current handling capability due to an increase in $V_{CE(sat)}$ and possible associated latching problems.

Figure 9: Behavior In Turn-Off With Inductive Load



SAFE OPERATING AREA -SOA

The SOA of an IGBT can be divided into three main areas, distinguished by current and voltage as indicated in the table below.

Table 1: Voltage Current Physical Limit

	Voltage	Current	Physical Limit
Zone 1	High	Low	Breakdown Voltage
Zone 2	Low	High	Latch up
Zone 3	High	High	Power Dissipation

The 3 zones are easily recognizable in figure 10.

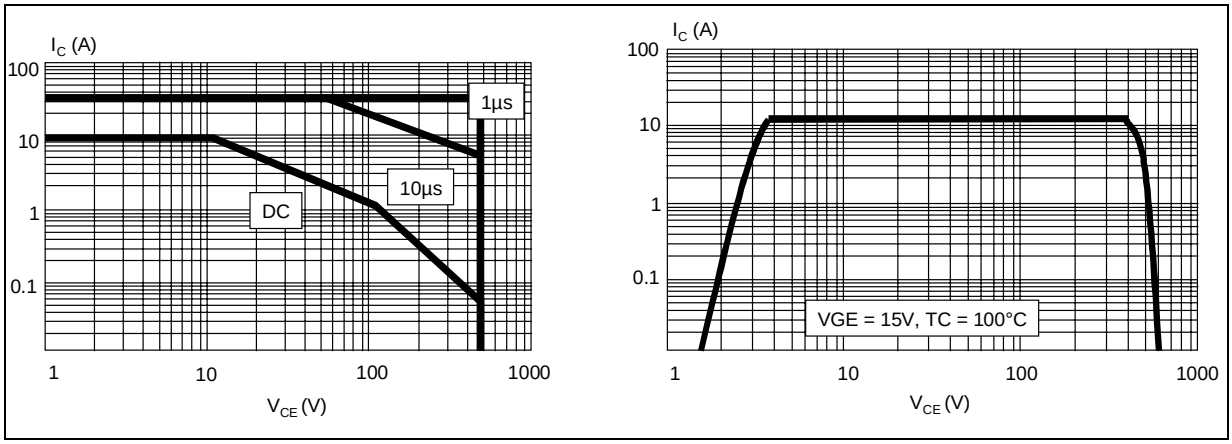
The curves describing robustness in forward conduction (Forward Bias Safe Operating Area, FBSOA), in reverse (Reverse Bias Safe Operating Area, RBSOA), and in short circuit (Short Circuit Safe Operating Area, SCSOA) are usually available in every datasheet.

More in detail:

FBSOA

This part of the SOA represents the region where both electron and hole current flows during the turn on transient. The physical limit is given by the maximum voltage the device can withstand when the I_C is saturated, as indicated in figure 10.

Figure 10: SOA



RBSOA

This region represents the turn off transient, when the gate bias is zero or negative but I_C is still present as the hole current is not extinguished. Here the parasitic transistor, described before, can start the latch up if the current increases too much. When this occurs, the device can no longer be controlled by the gate. The latest IGBTs do not exhibit this type of behavior, since the triggering of this parasitic SCR can be made to occur at a current much higher than the one encountered in normal operation (typically I latch> 5 I_C nominal) with appropriate modifications to the structure and the process. Figures 11 and 12 show the variation in latch current as a function of junction temperature and gate resistance respectively.

Figure 11: Variation Of Latching Current I_{latch} With Temperature

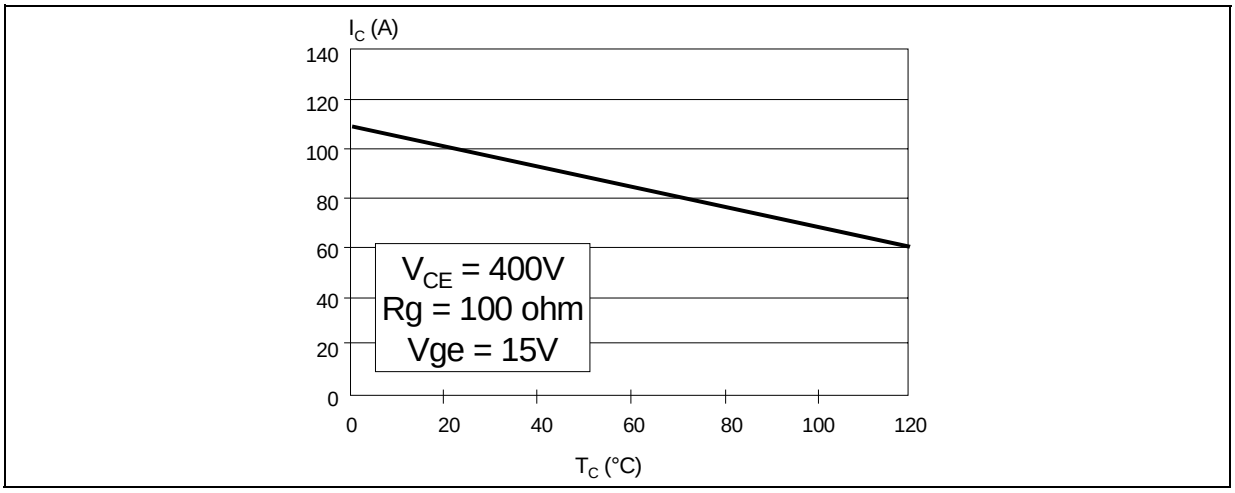
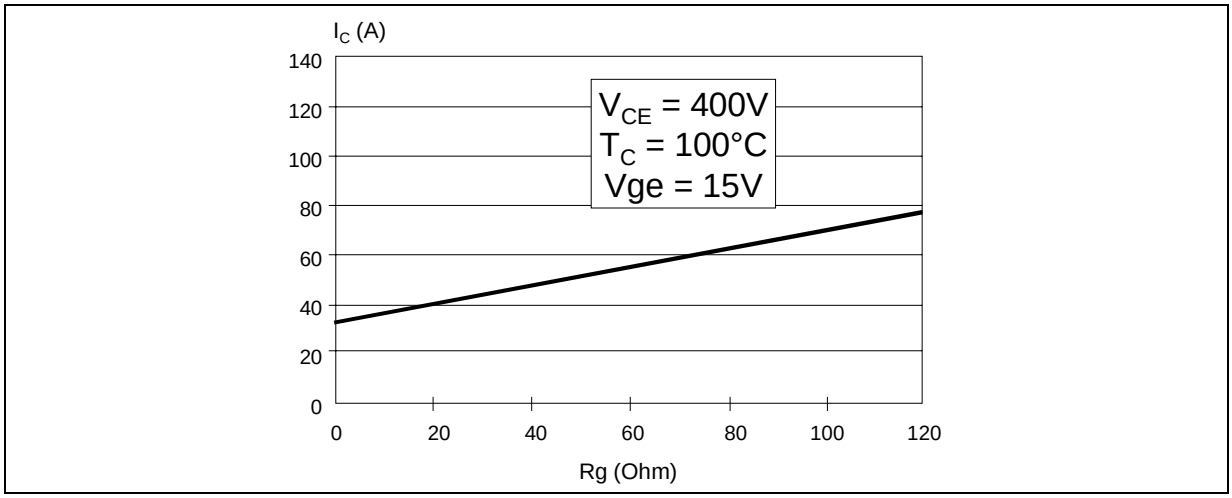


Figure 12: Variation Of Latching Current I_{latch} With Rg

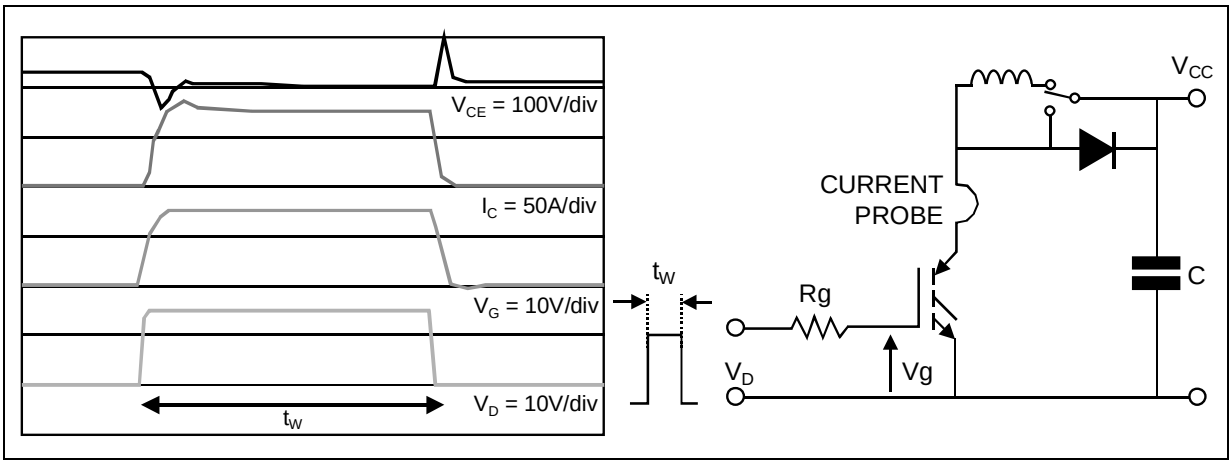


SCSOA

This is measured by turning on the device at the supply voltage and measuring the maximum time during which the drive circuit can control the device under test. Figure 13 shows the waveform and the off time for three devices with equivalent characteristics but manufactured using different technologies.

10. MAXIMUM OPERATING FREQUENCY.

Figure 13: Short Circuit Test



The switching frequency is a very important parameter when choosing a proper IGBT. This is important since it is strictly related to the power losses of the device. For this reason all silicon producers have different families tailored for working at different switching frequencies.

In particular STMicroelectronics at the moment offers two different series of products (H, S types), but other families are in development (K, F, L), giving the customer the possibility to choose the best trade off in terms of total power losses associated to conduction and switching phases.

In particular it is possible to define the conduction losses as the power dissipated when the current flows

and mainly related to $V_{CE(sat)}$.

They could be expressed as: $\mathbf{P_{cond} = V_{CE} * I_C * \delta}$ where δ is duty cycle

The switching losses are the related to the IGBT's commutation, they are mainly associated with the total energy dissipated in operation E_{ts} and strictly dependent from the frequency f of the end equipment:

$P_{sw} = E_{ts} * f$

The total losses are the sum of the two parts:

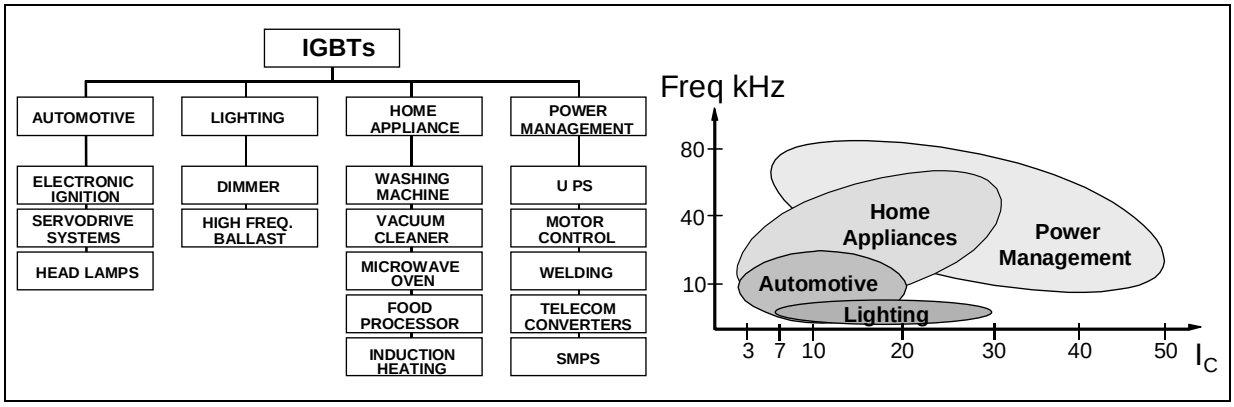
$\mathbf{P_{tot} = P_{cond} + P_{sw}}$

At this point it is clear that the overall power dissipation is intrinsically related to two main parameters E_{ts} and $V_{CE(sat)}$.

The right trade off between these two variables, strictly related to the IGBTs technology, offers the customer the option to minimize the overall heat dissipation of the end equipment.

So depending on the frequency of the end equipment and the current level features intrinsically dependent on application specifications, different parts are chosen in order to minimize the power consumption.

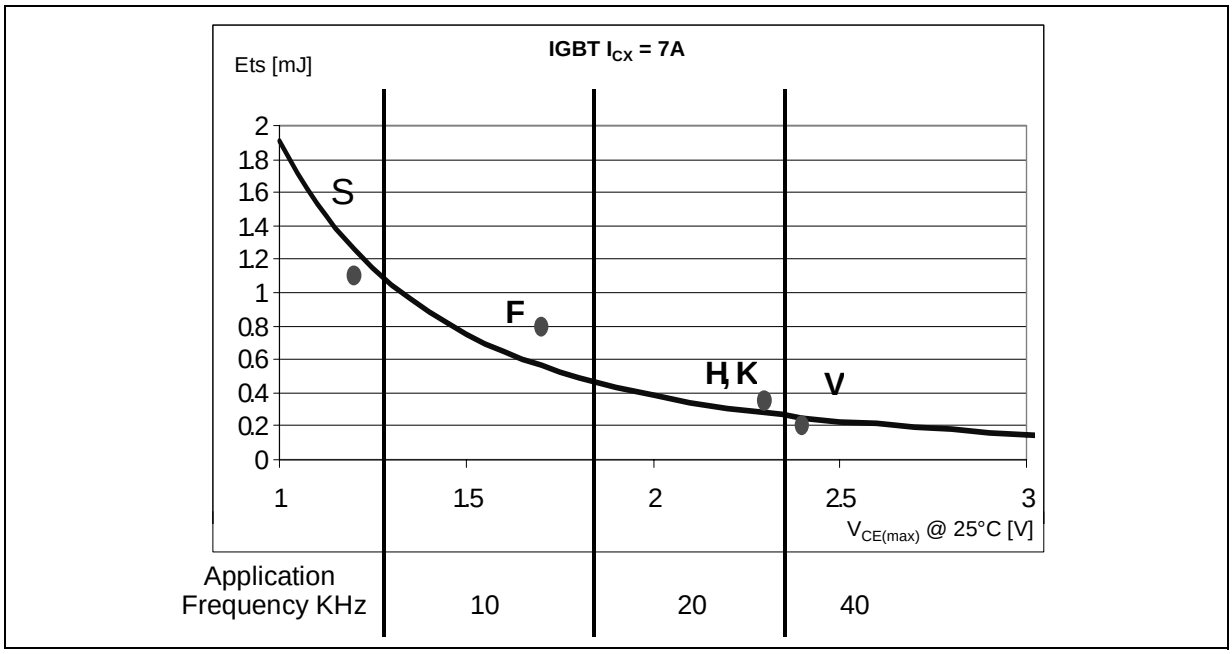
Figure 14: Main Cluster For End Equipment



STMicroelectronics represents, especially at current level ideals for motor control, the best trade off between E_{ts} and $V_{CE(sat)}$, as shown in the chart below. Moreover, the dopant typology used allows a decrease in $V_{CE(sat)}$ with the temperature rise, giving a further advantage during the use of the device.

More than this, STMicroelectronics is now developing new families with different trade off between E_{ts} and $V_{CE(sat)}$. A broader range of product is being offered in order to offer our customers and partners true independence in design criteria.

Figure 15: Trade-Off $V_{CE(sat)}$ - E_{ts}



11. DATA SHEET MAIN PARAMETERS.

11.1 Electric Parameters.

I_C -collector current

The maximum DC current can flow in the devices at a rated temperature (typically 100°C and 25°C).

Icm -pulsed collector current

The peak of the collector current can flow without exceeding maximum junction temperature. This parameter is strictly related to pulse width, duty cycle and thermal conditions of the device.

Ices -collector cut off current

Maximum collector-emitter leakage current with gate and emitter shorted, under a rated V_{CE} value (usually given @25C and @125C).

Iges –gate emitter leakage current

Maximum gate-emitter leakage current with collector and emitter shorted, under a rated Vge value.

Vces –collector emitter voltage

Maximum voltage between collector and emitter, with gate short-circuited with the emitter. This voltage indicates the physical limit related to the breakdown of the junction between the power terminals.

VBRces -collector emitter breakdown voltage

Breakdown voltage between collector and emitter with gate terminal shorted to the emitter one. This parameter is given at a rated current I_C.

Vge -gate emitter voltage

Maximum applicable voltage between gate and emitter.

Vgeth -gate emitter threshold voltage

Gate emitter voltage necessary to reach a specified I_C.

$V_{CE(sat)}$ –collector emitter saturation voltage

Collector emitter voltage with a fixed Vge (in general 15V) and for a rated value of collector current. This

voltage is usually indicated with Ic flowing in the device at 25°C and 100°C and it represents the voltage drop for the rated I_C.

11.2 Equivalent Capacitances.

Cies -input capacitance

Input capacitance with collector and emitter shorted.

Coes -output capacitance

Output capacitance with gate and emitter shorted.

Cres-reverse transfer capacitance

Collector and gate capacitance.

11.3 Time Parameters.

Tf -fall time
Time requested to reach 10% of the collector nominal current from 90% of its value. This parameter is fundamental for the understanding of the device's speed.

Tr -rise time

Time requested to reach 90% of the collector nominal current starting from 10% of its value.

Tdon -turn-on delay time

The time it takes for the collector current to reach 10% of nominal current value starting from the time a forward pulse is applied to the gate.

Tdoff -turn off delay time

The time it takes for V_{CE} to reach 10% of the rated value when the voltage's signal is removed from the gate.

Tsc-short circuit withstand time

This is the time an IGBT can resist without any permanent damage to the passage of a high value of current when V_{CC}=Vces/2, like in the condition of a short circuit in a motor control system. The minimum value generally requested for a short circuit series is 10µs.

11.4 Power Losses Indicators.

Eon –turn on switching losses

Total amount of energy lost during the turn-off with inductive load. The time interval considered starts when I_C rises from zero up to the time V_{CE} decreases to zero. It includes also diode losses when inserted in co-package.

Eoff –turn off switching losses

Total amount of energy lost during the turn off with inductive load. The time interval considered starts when V_{CE} rises from zero up to the time I_C decreases to zero. It also includes diode losses when inserted in co-package.

Ets –total switching losses

Total amount of energy lost during the switching. It is the sum of Eon and Eoff.

P_{tot} –maximum power dissipation

The maximum power dissipation esteemed when the Tj is at the maximum rated value.

11.5 Thermal Parameters.

Tj -junction temperature

Temperature of the junction. Industry standard range is from -55°C to 150°C.

Tstg –storage temperature

Temperature range for storage and transportation. Industry standard range is from -55°C to 150°C.

Rθjc-Thermal junction to case resistance

Thermal resistance between junction and package. When a diode is present, in the datasheet two values of Rθjc are indicated, one for the diode and another one for the IGBT.

Rθcs-Thermal case to sink resistance

Thermal resistance between case and sink. It varies with several parameters mainly related to materials and assembly systems.

Rsa-Thermal sink to ambient resistance

Thermal resistance between heatsink and ambient.