Application Note 9016 February, 2001

IGBT Basics 1

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Rev. A2, February 2001

1. Introduction

Prior to the development of the IGBTs (insulated gate bipolar transistor), power MOSFETs were used in medium or low voltage applications which require fast switching. Whereas bipolar power transistors, thyristors and GTOs were used in medium to high voltage applications which require high current conduction. A power MOSFET allows for simple gate control circuit design and has excellent fast switching capability. On the other hand, at 200V or higher, it has the disadvantage of rapidly increasing on-resistance as the breakdown voltage increases. The bipolar power transistor has excellent on-state characteristics due to the low forward voltage drop, but its base control circuit is complex, and fast switching operation is difficult as compared with the MOSFET. The IGBT developed in the early 1980s has the combined advantages of the above two devices. It has a MOS gate input structure, which has a simple gate control circuit design and is capable of fast switching up to 100kHz. Additionally, because the IGBT output has a bipolar transistor structure, its current conduction capability is superior to a bipolar power transistor. Based upon these excellent characteristics, the IGBT has been extensively used in applications exceeding 300V voltage as an alternative to power MOSFETs and bipolar power transistors. Its area of application continues to increase. The IGBT is becoming more modular as its use increases in applications that require higher current conduction capability.

History of the Fairchild IGBT

Fairchild Semiconductor began developing the IGBT in 1992. This was later than its competitors for a power semiconductor company. However, Fairchild Semiconductor was able to catch up with its leading competitors with the development of the third generation 600V IGBT and 1500V ultra-fast IGBT for 220V power IH applications in 1995. In 1996, Fairchild Semiconductor developed the 600V rugged type RUF series with its own stripe pattern. This has strengthened short circuit withstanding capability, which makes it suitable for motor control applications such as inverters. Following this development, Fairchild Semiconductor used trench technology in 1998 to develop the 400V IGBT for camera strobes and the 900V IGBT for 110V power IH applications. Both of these require low-loss high current conduction capabilities. These design achievements indicated that Fairchild Semiconductor now possessed both planar and trench technologies. In particular, Fairchild has achieved world-class quality in 1998 by developing 1200V IGBT using SDB (silicon direct bonding) technology. Fairchild began research on SDB in 1996. Unlike existing technology, which uses an epi-grown wafer, SDB technology binds P^+ substrate and N^- substrate directly to allow easier manipulation of the thickness of the N^- substrate. This enables easier fabrication of high voltage IGBTs. Specifically, as the formation of a high density N^+ buffer layer is possible, fast switching characteristics can be obtained without high density electron irradiation, which increases the leakage current and decreases reliability. Hence, it enables the production of high speed, highly efficient and reliable IGBTs. It is also suitable for large capacity drives, as it has the same temperature characteristics as the NPT IGBT, which is suitable for a parallel drive. In the year 2000, Fairchild has applied this technology to develop 1500V and 1700V IGBTs. These can be used in 220V 1ϕ IH applications. Now, Fairchild is in the process of developing IPMs (Intelligent Power Modules), which are IGBT Inverter Modules that combine the control ICs in order to provide a lot of intelligent functions. The IPMs will drastically change the three-phase AC/DC Motor Speed Control arenas paving the way for reliable, compact and high performance designs.

2. Device structure and operation

2-1. Structure

The IGBT combines the advantages of a power MOSFET and a bipolar power transistor. Similarly its structure is a combination of the two devices. As shown in Fig. 1, the input has a MOS gate structure, and the output is a wide base PNP transistor. The base drive current for the PNP transistor is fed through the input channel. Besides the PNP transistor, there is an NPN transistor, which is designed to be inactivated by shorting the base and the emitter to the MOSFET source metal. The 4 layers of PNPN, which comprises the PNP transistor and the NPN transistor form a thyristor structure, which causes the possibility of a latch-up. Unlike the power MOSFET, it does not have an integral reverse diode that exists parasitically, and because of this it needs to be connected with the appropriate fast recovery diode when needed.

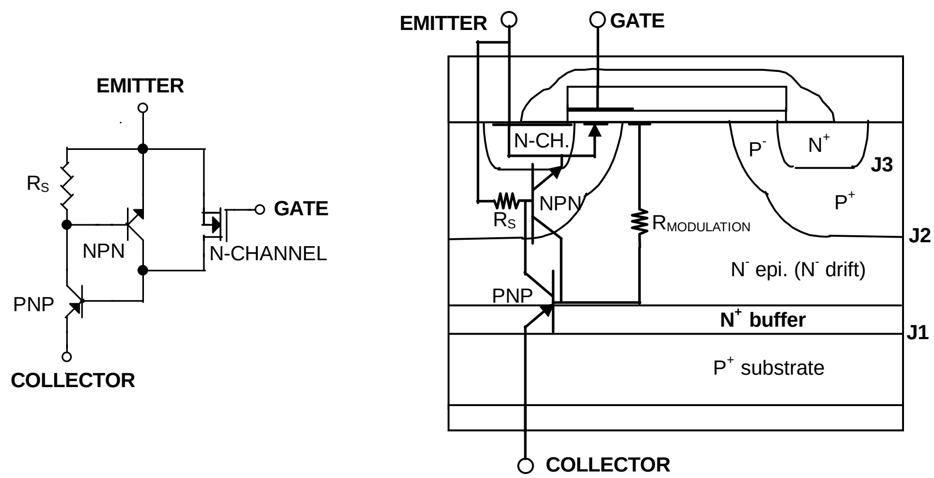


Figure 1. Equivalent Circuit for the IGBT & a Cross Section of the IGBT Structure (PT & N-Channel)

PT & NPT

An IGBT is called a PT (punch-through) or asymmetrical when there is an N^+ buffer layer between the P^+ substrate and N^- drift region. Otherwise, it is called an NPT (non-punch-through) IGBT or symmetrical IGBT. The N^+ buffer layer improves turn-off speed by reducing the minority carrier injection quantity and by raising the recombination rate during the switching transition. In addition, latch-up characteristics are also improved by reducing the current gain of the PNP transistor. The problem is that the on-state voltage drop increases. However, the thickness of the N^- drift region can be reduced with the same forward voltage blocking capability because the N^+ buffer layer improves the forward voltage blocking capability. As a result, on-state voltage drop can be lowered. Hence, the PT-IGBT has superior trade-off characteristics as compared to the NPT-IGBT in switching speed and forward voltage drop. Currently, most commercialized IGBTs (Fairchild IGBTs) are PT-IGBTs. Section (3-3) about static blocking characteristics illustrates that IGBT forward and reverse blocking capability are approximately equal because both are determined by the same N^- drift layer thickness and resistance. The reverse-blocking voltage of PT-IGBTs that contain N^+ buffer layer between P^+ substrate and N^- drift region is lowered to tens of volts due to the existence of a heavy doping region on both sides of J1.

2-2. Operation

Turn-on

When the device is in the forward blocking mode, and if the positive gate bias (threshold voltage), which is enough to invert the surface of P-base region under the gate, is applied, then an n-type channel forms and current begins to flow. At this time the anode-cathode voltage must be above 0.7V (potential barrier) so that it can forward bias the P^+ substrate / N^- drift junction (J1). The electron current, which flows from the N^+ emitter via the channel to the N^- drift region, is the base drive current of the vertical PNP transistor. It induces the injection of hole current from the P^+ region to the N^- base region. The conductivity modulation improves because of this high level injection of the minority carrier (hole). This increases the conductivity of the drift region by a factor varying from ten to hundred. This conductivity modulation enables IGBTs to be used in high voltage applications by significantly reducing the drift region resistance. There are two kinds of currents flowing into the emitter electrode. One is the electron current (MOS current) flowing through the channel, and the other is the hole current (bipolar current) flowing through the P^+ body / N^- drift junction (J2).

Turn-off

The gate must be shorted to the emitter or a negative bias must be applied to the gate. When the gate voltage falls below the threshold voltage, the inversion layer cannot be maintained, and the supply of electrons into the N^- drift region is blocked, at which point, the turn-off process begins. However, the turn-off cannot be quickly completed due to the high concentration minority carrier injected into the N^- drift region during forward conduction. First, the collector current rapidly decreases due to the termination of the electron current through the channel, and then the collector current gradually reduces, as the minority carrier density decays due to recombination.

3. Basic Characteristics

3-1. Advantages, Disadvantages and Characteristic Comparison with BJT and MOSFET

Advantages

(1) High forward conduction current density and low on-state voltage drop:
The IGBT has a very low on-state voltage drop due to conductivity modulation and has superior on-state current density compared to the power MOSFET and bipolar transistor. So a smaller chip size is possible and the cost can be reduced.

(2) Low driving power and a simple drive circuit due to the input MOS gate structure:
The IGBT can easily be controlled as compared to current controlled devices (thyristor, BJT) in high voltage and high current applications.

(3) Wide SOA:
With respect to output characteristics, the IGBT has superior current conduction capability compared with the bipolar transistor. It also has excellent forward and reverse blocking capabilities.

Disadvantages

(1) Switching speed (less than 100kHz) is inferior to that of the power MOSFETs, but it is superior to that of the BJT. The collector current tailing due to the minority carrier causes the turn-off speed to be slow.

(2) There is the possibility of latch-up due to the internal PNPN thyristor structure.

The Characteristics Comparison with a BJT and a MOSFET

Table 1: The IGBT Characteristics Comparison with BJT, MOSFET

Features	BJT	MOSFET	IGBT
Drive Method	Current	Voltage	Voltage
Drive Circuit	Complex	Simple	Simple
Input Impedance	Low	High	High
Drive Power	High	Low	Low
Switching Speed	Slow (μs)	Fast (ns)	Middle
Operating Frequency	Low (less than 100kHz)	Fast (less than 1MHz)	Middle
S.O.A.	Narrow	Wide	Wide
Saturation Voltage	Low	High	Low

3-2. Latch-up

The IGBT contains a parasitic PNPN thyristor structure between the collector and the emitter. A latch-up means the turning on of the thyristor. When there is action by a thyristor, the IGBT current is no longer controlled by the MOS gate. The IGBT would be destroyed because of excessive power dissipation produced by the amount of current over the rated value between the collector and the emitter.

Causes of latch-up

(1) Static latch-up mode:
Since the conductivity of the drift region under the gate electrode is increased by the introduction of electron current through the channel, most of the holes injected into the drift region are injected at the P body region under the channel and flow to the source metal along the bottom of N^+ source. Due to this, the lateral voltage drops across the shunting resistance (R_S, refer to Fig. 1) of the P body layer. If this voltage drop becomes greater than the potential barrier of the N^+ source / P body layer junction (J3), electrons are injected from the N^+ source to the P body layer, and the parasitic NPN transistor (N^+ source, P body and N^- drift) is turned-on. If the sum of the two NPN, PNP parasitic transistors' current gain becomes 1 ($\alpha_{NPN} + \alpha_{PNP} \geq 1$), latch-up occurs.

(2) Dynamic latch-up mode:
When the IGBT is switched off, the depletion layer of the N^- drift / P body junction (J2) is abruptly extended, and the IGBT latches up at a current lower than 1/2 of the static latch-up current due to the displacement current. And because of this, the safe operating area is limited.

Avoidance of latch-up

The first method is to prevent the NPN parasitic transistor from turning on, and the second is to keep the sum of the two NPN, PNP parasitic transistors' current gain less than 1 ($\alpha_{NPN} + \alpha_{PNP} < 1$) when the NPN parasitic transistor is turned on. In the latter case, the two transistors' current gain must be reduced. As the current gain is proportional to the base transport factor and the injection efficiency of an emitter-base junction, both must be reduced. In the PNP transistor, electron irradiation and the inserting of a N^+ buffer layer between the P^+ substrate and N^- drift region can be used, but it is difficult to reduce the current gain in the NPN transistor. So the following representative methods to improve latch-up characteristics are focused on preventing the turn-on of the NPN parasitic transistor.

(1) Application of P^+ body
This method is applied to most MOS gate power devices. In addition to the body, a highly doped P^+ region is formed in the middle of the body, and it covers most of the bottom part of source. When the doping concentration of the P^+ region is excessively raised to improve latch-up characteristics, the P^+ region affects the threshold voltage by diffusing the channel region and debase the forward characteristics.

(2) Cushion structure p^+ Double Implantation:
When using a highly doped P^+ body, there are limitations in lowering the resistance of the bottom part of N^+ source as the doping concentration of the P^+ body reduces horizontally due to diffusion. Ion is first injected to form the N^+ source. Then high energy p+ ion is injected, and it is put through a thermal process to form P^+region at the bottom of the N^+ source. Fairchild is producing latch-up proofed IGBTs by applying this method and EBR (Emitter Ballast Resistor: further explained in (6)).

(3) Application of short N^+ source:
This method reduces the resistance at the bottom of the N^+ source.

(4) Reduction of the hole current:
The voltage drop across the bottom of the N^+ source can be reduced by reducing the hole current passing through the P body. Inserting the highly doped N^+ buffer, reducing the space between P bodies, and reducing the current gain by electron irradiation are the methods to reduce the hole current.

(5) Minority Carrier By-Pass:
The minority carrier by-pass design has two hole current paths. One is a normal path and the other flows to the emitter contact directly without passing through the bottom of the N^+ emitter. So the hole current flowing through the bottom of the N^+ emitter is reduced to half, and the latching current density doubles. In spite of an increase in the on-state voltage drop, this method is widely used because it enables safe operation without latch-up phenomenon at higher current and temperature.

(6) Layout:
The latch-up characteristics can be improved by changing the N^+ source's cell structure on the surface of the device. Generally, a linearly structured cell has worse forward current conduction characteristics than a cellularly structured cell, but shows better latch-up characteristics. A MSS (multiple surface short) structure with better latch-up characteristics as compared to the linear structure has also been developed. There is another method (EBR) used in Fairchild IGBTs, which increases the voltage drop level across the bottom of N^+ source that forward biases the emitter (N^+ source region)-base (P body region) junction (J3). This is done by making the voltage drop inside the N^+ source by changing the length of the N^+ source.

(7) Others:
There is also a method to build in a sense IGBT cell and protection devices. This limits the current by reducing the gate voltage automatically, when the current flows over a certain limit. If a large series gate resistance R_G is used when the IGBT is applied to a certain set, the turn-off speed is slowed and the diffusion speed of the depletion region of the drift region also slows down. Hence, the dynamic latch-up can be prevented. IGBTs currently under production have the latch-up proof characteristics.

High temperature characteristics (latching current density)

With a rise in temperature, the current gains of the NPN and PNP transistors increase. This decreases the latching current. The effect is aggravated by an increase in the resistance of the P base region due to a decrease in hole mobility.

3-3. Static Blocking Characteristics

Reverse Blocking Capability

When negative voltage is introduced to the collector as shown in Fig. 1, the P^+ substrate / N^- drift junction (J1) is reverse biased, and the depletion layer generally expands to the N^- drift region. As such, securing an optimal design in resistivity and thickness for the N^- drift region is essential in obtaining desirable reverse blocking capability. As a general guideline, the width of the N^-drift region is equivalent to the sum of depletion width at maximum operating voltage and minority carrier diffusion length. It is important to optimize the breakdown voltage while maintaining a narrow N^- drift region width, as the forward voltage drop increases with an increase in N^- drift region width. The following is an equation for calculating the N^- drift region width:

$$d_1 = \sqrt{\frac{2\varepsilon V_m}{qN_D}} + L_p$$

where, d_1: N-drift region width
V_m: maximum blocking voltage
N_D: doping concentration
L_p: minority carrier diffusion length

Forward Blocking Capability

When the gate is shorted at the emitter, and a positive voltage is introduced at the collector, the P base / N^- drift region junction (J2) is reverse biased, and it is supported upto the rated voltage by the depletion region formed at the N^- drift region.

3-4. Leakage Current

Leakage current is divided into two types. One is leakage current from the depleted drift region, and the other flows on the surface of the junction termination. Since the IGBT uses a P^+ substrate and is irradiated with electrons to improve switching speed, the amount of leakage current from the drift region is greater than that of the power MOSFET. If there is a high voltage between the anode and cathode when the IGBT is off, the depletion region widens to nearly the entire drift region from the P^+ body / N^- drift junction (J2), and the entire region becomes depleted. The electron hole created by the heat of the depletion region is manifested as leakage current according to the area of the depletion region and minority carrier lifetime. This increases with the increase of the rated voltage and current. In particular, leakage current increases as the minority carrier lifetime shortens. As such, leakage current tends to increase with higher speed IGBTs.

3-5. Forward Conduction Characteristics

Due to its structure, the IGBT is sometimes viewed as a serial connection of the MOSFET and PiN diode, and sometimes it is seen as a wide base PNP transistor driven by the MOSFET in Darlington configuration. The former description can be used to understand the behavior of the device, but the latter better describes the IGBT.

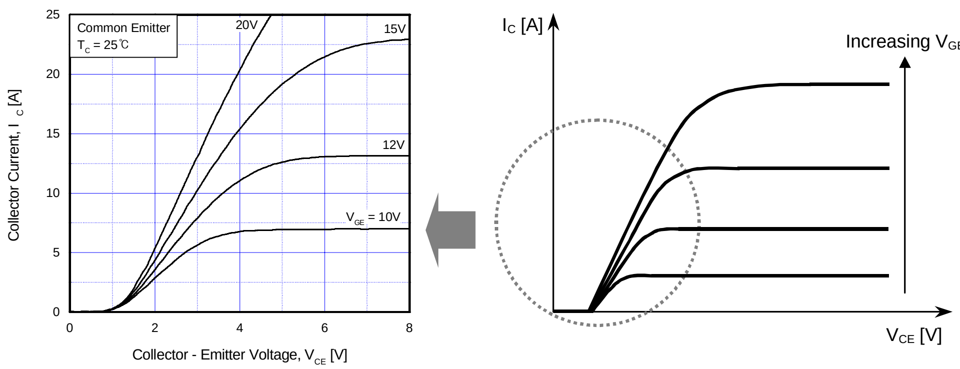


Figure 2. Static Characteristics of the IGBT

Fig. 2 is a graph of the IGBT's static characteristics. Even if a MOSFET channel of the input side is formed, the collector current does not flow if the anode-cathode forward voltage drop does not exceed approximately 0.7V as in the PiN diode. In addition, the current is saturated when the voltage across the MOSFET channel is greater than ($V_{GE} – V_{th}$) and has an infinite output resistance, as in a power MOSFET. However, in a symmetrical IGBT, the collector current increases with the increase in collector voltage, and the rate of increase in the collector current also increases with the increase in collector voltage. Such finite output resistance is due to a shortening of the channel due to an increase in the collector voltage, and a secondary decrease in the drain output resistance due to bipolar transistor current flow. In order to increase the collector output resistance, an asymmetrical structure with a N^+ buffer layer between the N^- drift region and P^+ substrate is used to prevent an increase in the bipolar transistor's current gain with the increase in the collector voltage. In an asymmetrical structure, the width of the undepleted N^- drift region does not change rapidly with the increase in the collector voltage due to the high concentration of the buffer layer, but it remains the same width as the N^+ buffer layer for all collector voltages. This results in a constant value of the PNP transistor's current gain. In addition to this, the N^+ buffer layer reduces the injection efficiency of the P^+ substrate / N^+ buffer junction (J1). This reduces the current gain of the PNP transistor. As such, an IGBT with an asymmetrical structure has much superior output characteristics than a symmetrical type. In addition, collector output resistance can be increased with electron irradiation to shorten the minority carrier lifetime, which reduces the diffusion length. The following is the equation for obtaining the saturated collector current of the IGBT:

$$I_{C,sat} = \frac{1}{(1-\alpha_{PNP})}\frac{\mu_{ns}C_{ox}Z}{2L_{CH}}(V_{GE}-V_{th})^2$$

where, μ_{ns}: surface mobility of electrons

C_{ox}: gate-oxide capacitance per unit area

Z: channel width

L_{CH}: channel length

V_{th}: threshold voltage

V_{GE}: applied gate voltage

Transconductance at the active region can be obtained by differentiating the $I_{C,sat}$ with respect to V_{GE}.

$$g_{fe} = \frac{1}{(1-\alpha_{PNP})}\frac{\mu_{ns}C_{ox}Z}{L_{CH}}(V_{GE}-V_{th})$$

The IGBT's saturated collector current and transconductance are higher than those of the power MOSFETs of the same aspect ratio (Z/L_{CH}). This is because the PNP transistor's current gain (α_{PNP}) is less than 1 (0.2 to 0.3 in general).

On-state voltage drop

Forward current-voltage characteristics and the conduction loss of a MOSFET are described as on-resistance. On the other hand, the characteristics of the IGBT are described as voltage drop at rated current, as is the case with the bipolar power transistor. On-state voltage drop is comprised of voltage drop of the forward biased P^+ substrate / N^- drift junction (J1), the voltage drop of conductivity modulated N- drift region and the voltage drop of MOSFET. Cut-in voltage for forward biased J1 is about 0.7V at room temperature. Cut-in voltage decreases due to a sharp increase in intrinsic carrier concentration as the temperature rises. The voltage drop of the N drift region can be obtained by integrating the electric field of the entire drift region, and it is generally less than 0.1V due to a strong conductivity modulation caused by injected holes from J1. The voltage drop of a MOSFET is the sum of the voltage drops from the channel region, JFET region and accumulation layer. Due to a decrease in drift layer resistance, the portion of JFET resistance and channel resistance is increased in the voltage drop between on-state collector-emitter. Hence, low JFET and channel resistance design are important factors in obtaining the best performance in an IGBT. The voltage drop at the channel is proportional to the channel length, gate oxide thickness. And it is inversely proportional to channel width, electron mobility and gate bias. The channel width can be increased by increasing the concentration of circuits by decreasing the size of each unit cell. But because of this the JFET resistance increases significantly, so the optimal size of the unit cell exists for each voltage rating. The IGBT decreases the minority carrier lifetime with electron irradiation in order to improve the switching speed, and this increases the on-state voltage drop. Even in IGBTs with the same structure, the IGBT with a fast switching speed has a larger voltage drop, and the IGBT with a slower switching speed has a smaller on-state voltage drop depending on the condition of electron irradiation, which takes place after device fabrication.

High temperature characteristics

One must be aware of the changes in characteristics from changes in temperature, as the IGBT's input characteristics are similar to a MOSFET, and output characteristics are similar to bipolar transistors. As temperature rises, the energy barrier of the P^+ substrate / N^- drift region junction (J1: emitter-base junction of PNP transistor) decreases, which leads to a lower cut-in voltage, and the threshold voltage decreases as in a MOSFET. As channel resistance increases, the amount of electron current (MOS current) decreases, which is injected to the N^- drift region. However, current gain, which is the ratio of the hole current (bipolar current) to the electron current, increases. In addition, N^- drift region (base of the PNP transistor) resistance increases. Due to these characteristics, changes in cut-in voltage of J1 are larger than those in channel resistance and N^- drift region resistance at low collector current level, so the IGBT has negative temperature coefficient similar to the bipolar transistor. On the other hand, channel resistance and N^- drift region resistance determine the on-state voltage at high collector current, which results in a positive temperature coefficient similar to a power MOSFET. The crossover point for the two characteristics is different for each product, and the collector-emitter voltage drop is independent from temperature at the crossover point. In real applications, it is used in areas with negative temperature coefficient, and these factors must be considered in parallel application. Figs. 3~5 illustrate these characteristics with graphs from the data sheet.

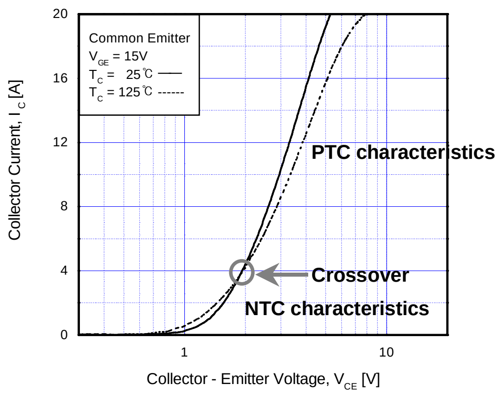


Figure 3. Typical Saturation Voltage Characteristics

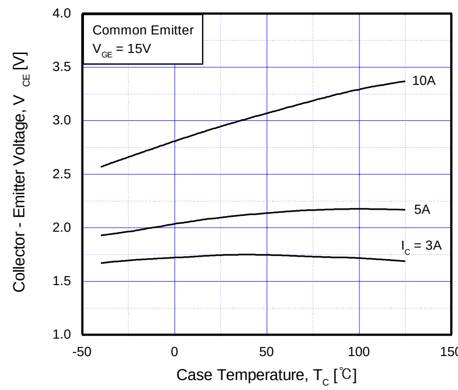


Figure 4. Saturation Voltage vs. Case Temperature at variant Current Level

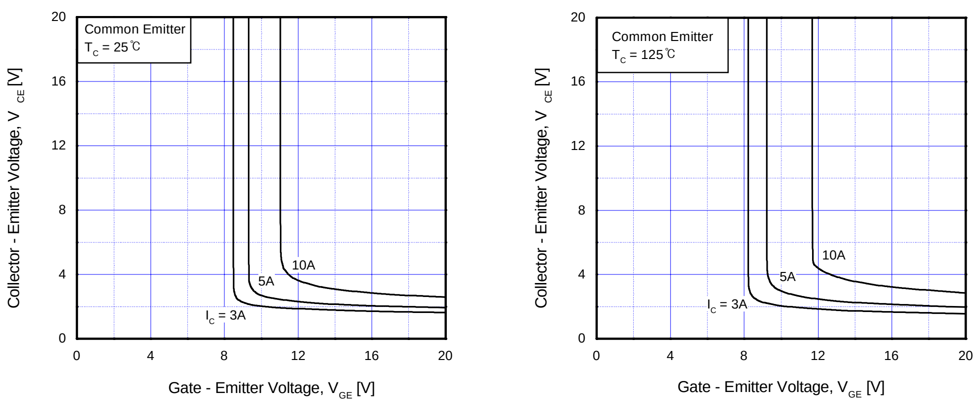


Figure 5. Saturation Voltage vs. V_{GE} due to Collector Current, Case Temperature

3-6. Switching Characteristics

Turn-on

When the device is in the forward blocking mode, and if the positive gate bias (threshold voltage), which is enough to invert the surface of P base region under the gate, is applied, then an n-type channel forms and the current begins to flow. At this time the anode-cathode voltage must be above 0.7V (potential barrier), so that it can forward bias the P^+ substrate / N^- drift junction (J1). The electron current flowing from the N^+ emitter to the N^- drift region through the channel is the base drive current of the vertical PNP transistor, and it induces a minority carrier (hole) injection from the P^+ region to the N^- base region. The current that flows to the emitter electrode are divided into the electron current (MOS current) flowing through the channel and bipolar current flowing through the P body / N^- drift junction (J2). When gate bias falls to near the threshold voltage at on-state, the inversion layer conductivity is reduced, and significant voltage drop that arises from electron current flow occurs across the region as in a MOSFET. When the voltage drop is equal to the difference between the gate bias and threshold voltage (V_{GE} - V_{th}), then the channel is pinched off. At this point, the electron current becomes saturated. Since this limits the base drive current of the PNP transistor, the hole current flowing through the PNP transistor is also limited. As a result, the device operates with saturated current at the active region (gate controlled output current).

Turn-off

The gate must be shorted to the emitter or a negative bias must be applied to the gate. When the gate voltage falls below the threshold voltage, the inversion layer cannot be maintained, and the supply of electrons into the N^- drift region is blocked. At this point the turn-off process begins. As illustrated in Fig. 6, the collector current (I_{CO}) falls to zero in two stages. As the electron current supplied through the MOSFET channel during the on-state is stopped, collector current suffers an initial abrupt fall (I_{CD}). After that, the tail current (I_{CT}) comes from the minority carrier (hole) that was injected through the N^- drift region from the P^+ substrate during the on-state. The tail current of the IGBT lowers switching characteristics and increases switching loss. Since N^- drift region is the base of the PNP transistor, it cannot be approached from outside, so it is not possible to control the tail current from outside. But it can be controlled with the amount of minority carrier (hole) injected through the N^- drift region and recombination rate when it is off. In order to reduce the amount of injected minority carrier and increase the recombination rate when it is off, the concentration and the thickness of the N^+ buffer layer between the P^+ substrate and N^- drift region must increase, as well as the dose of electron irradiation (in FSC, electron irradiation is applied to above 600V class except 400V) that takes place after device fabrication. However, improving the switching speed of the IGBT generally accompanies reduced current handling capability. As such, the trade-off between switching speed, which is related to switching loss, and forward voltage drop, which in turn is related to conduction loss, is important. The asymmetric structure is superior in such trade-offs as compared to a symmetric structure, and it can be improved by increasing the doping concentration in the buffer layer. In terms of power loss, the power MOSFET is better suited for lower blocking voltage and high operating frequency applications, while the IGBT is better suited for higher blocking voltage and lower operating frequency.

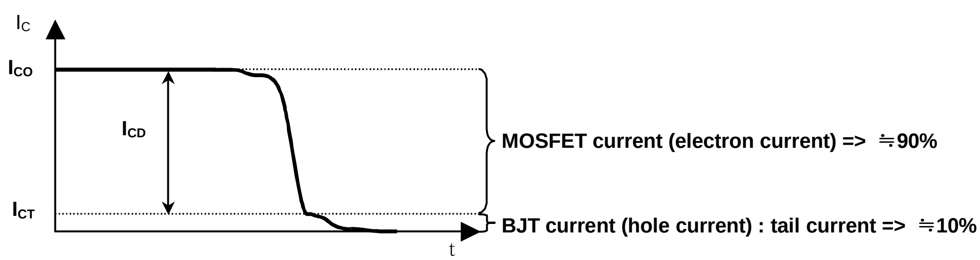


Figure 6. Collector Current During Turn-off

High temperature characteristics

The minority carrier lifetime in the drift region increases as the temperature increases. This not only delays recombination process (tail current) of the minority carrier, but it also increases the PNP transistor gain. So the portion of the initial abrupt fall (I_{CD}) in the overall collector current reduces. As such, t_f(fall time) of the spec is lengthened, and turn-off time increases with an increase in temperature, and the asymmetric structure has a lower rate of increase than the symmetric structure.

3-7. SOA (Safe-Operating-Area)

The SOA of an IGBT can be divided into the following three boundaries based on the stress conditions of voltage and current.

(1) High voltage, low current: Maximum voltage is limited by breakdown voltage.
(2) High current, low voltage: Maximum current is limited by latch-up of parasitic thyristor.
(3) Simultaneous high current and voltage: Limited by the rise in temperature caused by high power dissipation.

If the high current and voltage are introduced simultaneously for a short time, then the SOA is no longer limited by power dissipation. The following explanation illustrates the safe operating area for short duration simultaneous application of high current and voltage stress at the time of turn-on and turn-off of the IGBT with inductive load with FBSOA and RBSOA.

FBSOA (Forward Biased Safe-Operating-Area)

FBSOA indicates the safe operating region when both electron and hole current flow takes place along the high voltage on the device as positive gate bias is introduced on the IGBT during turn-on transient (Fig. 7). This is an important characteristic of an application with inductive load, and the IGBT has superior FBSOA without a snubber. The FBSOA of an IGBT is the maximum voltage the device can withstand without failure when the collector current is saturated. The limit can be obtained with the following equation:

$$\alpha_{PNP} M = 1$$

where, α_{PNP}: current gain of the PNP transistor

$$\alpha_{PNP} = \frac{1}{\cosh(1/L_a)}$$

where, l: undepleted N base width
L_a: ambipolar diffusion length
M: multiplication coefficient

$$M = \left[1 - \left(\frac{V}{BV_{SOA}}\right)^n\right]^{-1}$$

where, V: applied reverse bias supported by the junction
BV_{SOA}: avalanche breakdown voltage
n: 6 for a p^+n junction

It can be seen from the above formula that avalanche breakdown takes place at lower collector bias when the collector current increases. By reducing the doping concentration at the drift region, BV_{SOA}(breakdown voltage) can be raised, and this is possible in an asymmetrical structure, which does not have the danger of reach-through breakdown.

RBSOA (Reverse Biased Safe-Operating-Area, Turn-Off SOA)

RBSOA shows the safe operating area during the turn-off transient period, when the gate bias with positive value switches to zero or a negative value, which leaves the device with high voltage and hole current transport (refer to Fig. 8). Unlike the FBSOA, the snubber circuit design is important in the IGBT for safe operation during turn-off. A wider RBSOA can be obtained by reducing the current gain of the PNP transistor. The RBSOA of p-channel and n-channel IGBTs are compared under an identical doping profile and cell structure. The n-channel has a wider safe operating area for collector voltage (avalanche induced SOA limit) but a narrower safe operating area for collector current (current induced latch-up limit). It is the opposite for p-channel. The avalanche induced SOA limit is affected by the impact ionization coefficient of the carrier transported through the depletion layer. The n-channel IGBT has a superior avalanche induced SOA limit because the impact ionization coefficient of the hole transported in the n-channel IGBT is lower than that of the electron. Since N base region sheet resistance of the p-channel IGBT is about 2.5 times lower than the P base region sheet resistance of the n-channel IGBT, the p-channel IGBT is superior to the n-channel IGBT in current induced latch-up limit.

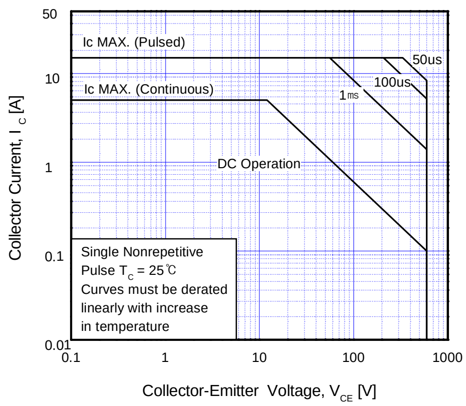


Figure 7. SOA Characteristic

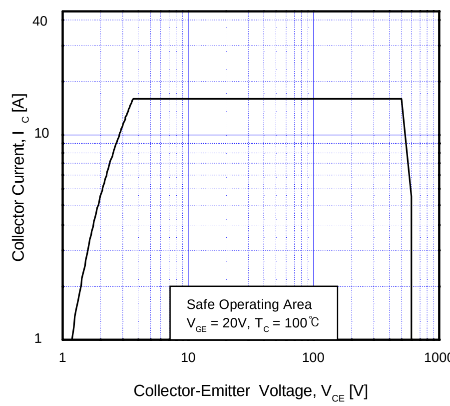


Figure 8. Turn-off SOA Characteristics

SCSOA (Short Circuit Safe-Operating-Area)

The system must be shut down to prevent the destruction of the device when the load shorts and allows excessive current, high voltage and high current to simultaneously put stress on the device. SCSOA defines the area of safe operation for the device under such fault condition.

4. Explanation of Data Sheet Parameters

4-1. Absolute Maximum Ratings

V_{CES} (Collector-Emitter Voltage)

It is the maximum allowable voltage between the collector and the emitter when the gate and the emitter are shorted. If this limit is exceeded, the device can be destroyed due to the breakdown of the junction between the collector and the emitter.

V_{GES} (Gate-Emitter Voltage)

It is the maximum voltage that can be introduced between the gate and the emitter. It is specified at 20V or 25V depending on the thickness and the characteristics of the gate oxide layer (or by product).

I_C (Collector Current @T_C=25°C and @T_C=100°C)

It is the maximum DC current the device can flow at the specified case temperature, and the calculation of I_C can be obtained from the following formula for calculating P_D.

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} = V_{ce} \times I_c \qquad [W]$$

The above formula can be restated with respect to I_c.

$$I_c = \frac{\sqrt{R_{\theta JC} \times VTO_{max}{}^2 + 4 \times R_{CE} \times (T_{J(max)} - T_C)}}{2 \times \sqrt{R_{\theta JC}} \times R_{CE}} - \frac{VTO_{max}}{2 \times R_{CE}} \qquad [A]$$

where, $R_{\theta JC}$: junction-to-case thermal resistance

T_C: case temperature

$T_{J(max)}$: maximum junction temperature

V_{CE}, R_{CE}, VTO_{max}: Refer to Fig. 9

$$V_{ce} = VTO + R_{CE} \times I_c$$

$$R_{CE} = \frac{\Delta V_{ce}}{\Delta I_c}$$

$$VTO_{max} = VTO + [V_{ce(sat),(max)} - V_{ce(sat),(typ)}]$$

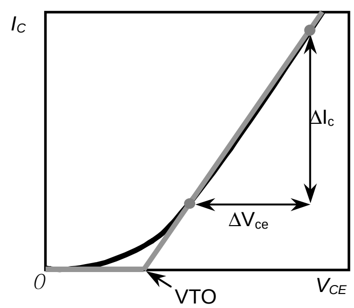


Figure 9. Linear Interpolation of output characteristics at T_j = 150°C

The specification is influenced by the device's ability to remove heat (heat resistance), and the current specification at the case temperature of 25°C represents the current rating of the device. The current specification at the case temperature of 100°C is more usable in real applications.

I_{CM} (Pulsed Collector Current)

** Repetitive rating: Pulse width limited by max. junction temperature*

It is the peak current the device can flow above the I_C specification under the maximum junction temperature. It varies with the current pulse width, duty cycle and the heat dissipation conditions.

I_F (Diode Continuous Forward Current @T_C=100°C)

It is the maximum DC current the diode can flow in the forward direction at the specified case temperature.

I_{FM} (Diode Maximum Forward Current)

It is the peak current the diode can flow above the I_F specification under the maximum junction temperature.

T_{SC} (Short Circuit Withstand Time @T_C=100°C)

Refer to the T_{SC} explanation of Electrical Characteristics of IGBT.

P_D (Maximum Power Dissipation @T_C=25°C, @T_C=100°C)

The maximum power dissipation value with the assumption that the junction temperature rises to the maximum rating at case temperatures of 25°C and 100°C.

$$P_D = \frac{T_{J(max)} - T_C}{R_{\theta JC}} \qquad [W]$$

T_J (Operating Junction Temperature)

The industry standard range is -55°C ~ 150°C, and the maximum junction temperature is 150°C.

T_{stg} (Storage Temperature Range)

It is the range of temperature for storage or transportation for the device, and it must be between -55°C ~ 150°C.

T_L (Maximum Lead Temp. for Soldering Purposes at 1/8 from case for 5 seconds)

It is the maximum lead temperature during soldering. The lead temperature must not exceed 300°C for 5 seconds at 1/8" from the case.

4-2. Thermal Characteristics

The power loss from the device turns into heat and increases the junction temperature inside the chip. This degrades the characteristics of the device and shortens its life. It is important to allow the heat produced from the chip junction to escape outside to lower the junction temperature. The thermal impedance $Z_{thjc}(t)$ measures the ability of the device to dissipate heat.

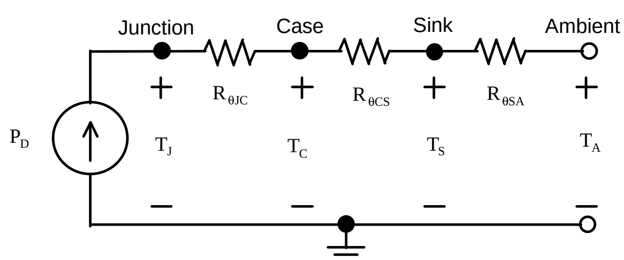


Figure 10. An Equivalent Circuit Based on Thermal Resistances

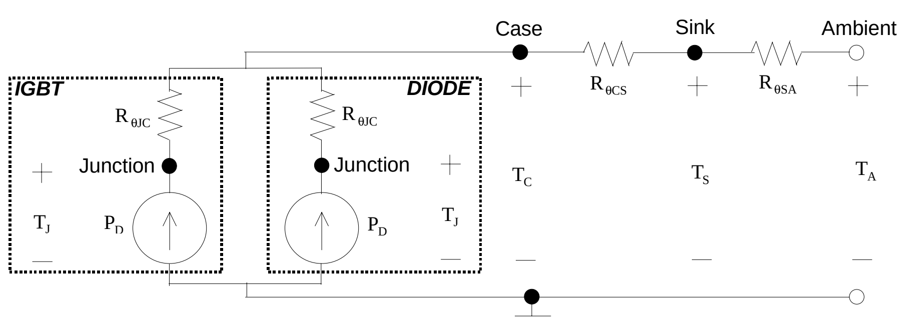


Figure 11. An Equivalent Circuit Based on Thermal Resistances (co-pak)

If the movement of heat is considered the same as current and it is changed to an electric circuit, the heat dissipation channel can be described as shown in Figs. 10 and 11 after considering thermal resistance. However, this is the case in DC operation, and most IGBT applications involve switching operations with a certain duty factor. In such cases, an equivalent circuit can be described with thermal impedance with consideration for thermal capacitance as well as thermal resistance (refer to the Thermal Response Characteristics section). The entire thermal resistance from the chip junction to ambient is denoted as $R_{\theta JA}$**(Thermal Resistance, Junction–to–Ambient),** and the following formula is for an equivalent circuit**.**

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad [°C/W]$$

$R_{\theta JC}$ (Thermal Resistance, Junction-to-Case)

It is the internal thermal resistance from the chip junction to the package case. This thermal resistance of a pure package is determined by the package design and lead frame materials. $R_{\theta JC}$ is measured under T_C = 25[°C] condition and can be described by the following formula.

$$R_{\theta JC} = \frac{T_J - T_C}{P_D} \qquad [°C/W]$$

T_C = 25[°C] is a condition with infinite heat sink.
* Infinite heat sink: Temperature of the package case is the same as the ambient temperature, it is a heat sink that can achieve $T_C = T_A$.

Co-pak products have specified the $R_{\theta JC}$ of IGBT and the $R_{\theta JC}$ of the diode, respectively.

$R_{\theta CS}$ (Thermal Resistance, Case–to–Sink)

It is the thermal resistance from the package case to the heat sink. It varies with the package, type of insulation sheet, the type of thermal grease and the thickness of its application, and the mounting method to the heat sink.

$R_{\theta SA}$ (Thermal Resistance, Sink–to–Ambient)

It is the thermal resistance from the heat sink to ambient, and it is determined by the geometric structure, surface area, cooling method and the quality of the heat sink.

Thermal Response Characteristics

Fig. 12 is derived from the Fig. 17 graph in the data sheet, and it illustrates $Z_{thjc}(t)$ (junction–to–case thermal impedance) with respect to changes in rectangular pulse duration under several duty factors. $Z_{thjc}(t)$ determines the peak junction temperature under the equation for peak $T_J = P_{dm} \times Z_{thjc} + T_C$ (Power dissipation during the conduction period is assumed to be constant at P_{dm} from Fig. 17 in the data sheet). As it approaches DC operation with a duty factor of D=1, and the rectangular pulse duration lengthens, $Z_{thjc}(t)$ is saturated at the maximum value of $R_{\theta JC}$. Fig. 13 illustrates that the junction temperature increases as the duty factor increases.

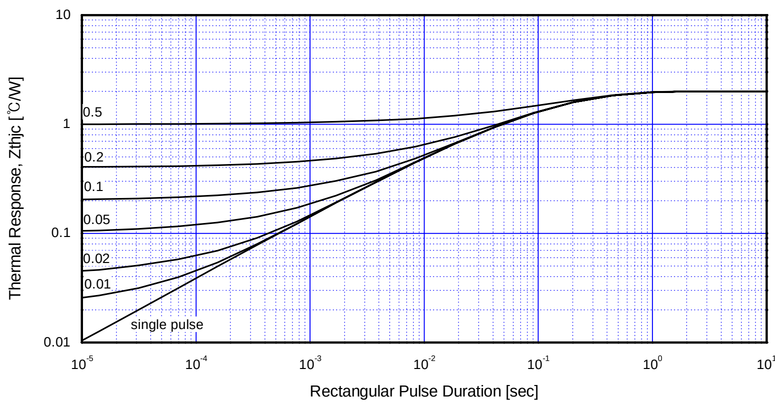


Figure 12. Transient Thermal Impedance of IGBT

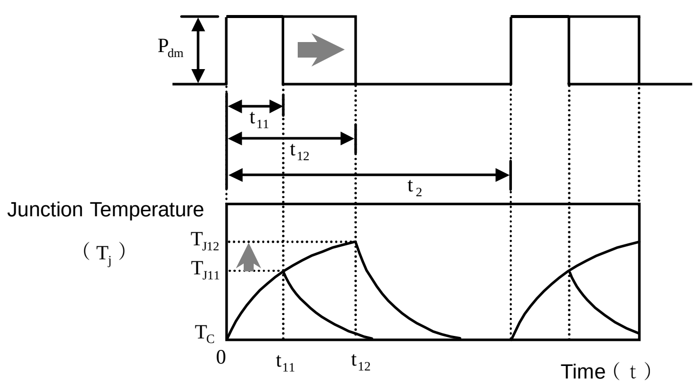


Figure 13. Changes in junction temperature respect to conduction time

A single pulse curve determines the thermal resistance for repetitive power pulses having a constant duty factor (D) as shown in the following equation.

$$Z_{thjc}(t) = R_{\theta JC} \cdot D + (1 - D) \cdot S_{thjc}(t)$$

where, $Z_{thjc}(t)$: Thermal impedance for repetitive power pulse with duty factor D
$S_{thjc}(t)$: Thermal impedance for single pulse

(4-3) Electrical Characteristics of the IGBT

Off Characteristics

BV_{CES} (Collector-Emitter Breakdown Voltage)

It is the breakdown voltage between collector and when the gate is shorted to emitter and a specified current flows.

ΔBV_{CES} / ΔT_J (Temperature Coefficient of Breakdown Voltage)

Collector-emitter breakdown voltage has positive temperature coefficient characteristics, and it generally increases by 0.6 [V/°C].

I_{CES} (Collector Cut-Off Current)

It is the maximum collector-emitter leakage current with the gate and the emitter shorted and with the introduction of rated collector-emitter voltage.

I_{GES} (G-E Leakage Current)

It is the maximum gate-emitter leakage current with the collector and the emitter shorted and with the introduction of rated gate-emitter voltage.

On Characteristics

$V_{GE(th)}$ (G-E Threshold Voltage)

It is the gate-emitter voltage at which collector current begins to flow. In the data sheet, it means the gate-emitter voltage that make the specified collector current flow.

$V_{CE(SAT)}$ (Collector to Emitter Saturation Voltage)

It is an important factor in determining the device's conduction loss, and it is the collector-emitter voltage drop when the collector current is at the rated value (I_C @T_C=25° and @T_C=100°C) and the gate-emitter voltage is V_{GE}=15V. When the collector current is low, it has negative temperature coefficient characteristics, and when the current is high, it has positive temperature coefficient characteristics.

Dynamic Characteristics

The capacitance of an IGBT is generally measured under specific conditions, and its decrease is inversely proportional to the bias voltage introduced in the collector-emitter as shown in Fig. 15. The datasheet specifies typical values under V_{GE} = 0V, f = 1MHz and V_{CE} = 30V.

C_{ies} (Input Capacitance)

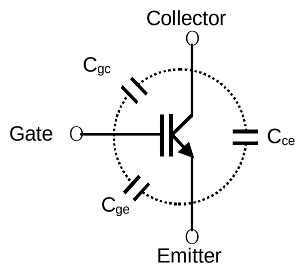
The input capacitance when the collector is shorted with the emitter.

C_{oes} (Output Capacitance)

The output capacitance when the gate is shorted with the emitter.

C_{res} (Reverse Transfer Capacitance)

The capacitance between the collector and the gate terminal.



$C_{ies} = C_{ge} + C_{gc}$, C_{ce} is shorted

$C_{res} = C_{gc}$

$C_{oes} = C_{ce} + C_{gc}$

Figure 14. Equivalent Circuit Showing Parasitic Capacitance

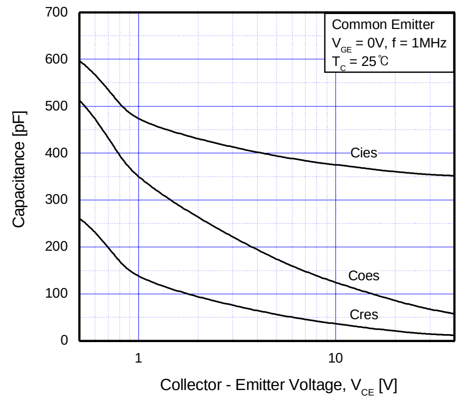


Figure 15. Capacitance Characteristics

Switching Characteristics

The diode-clamped inductive load circuit shown in Fig. 16 is a circuit commonly encountered in power electronics. It is a test circuit for switching characteristics. So with this circuit, we examine the IGBT's turn-on and turn-off behavior. Fig. 17 is a realistic switching waveform considering the characteristics of diode recovery and stray inductance (L_S). First, we set the condition to be in the constant steady state current, which initially flows through the inductive load and then flows through the ideal diode (freewheeling diode) connected in parallel with the inductive load.

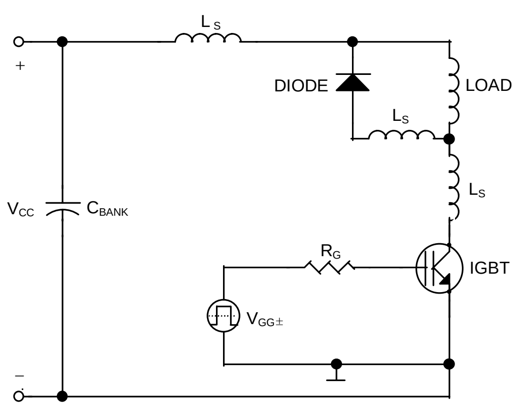


Figure 16. Diode-Clamped inductive load

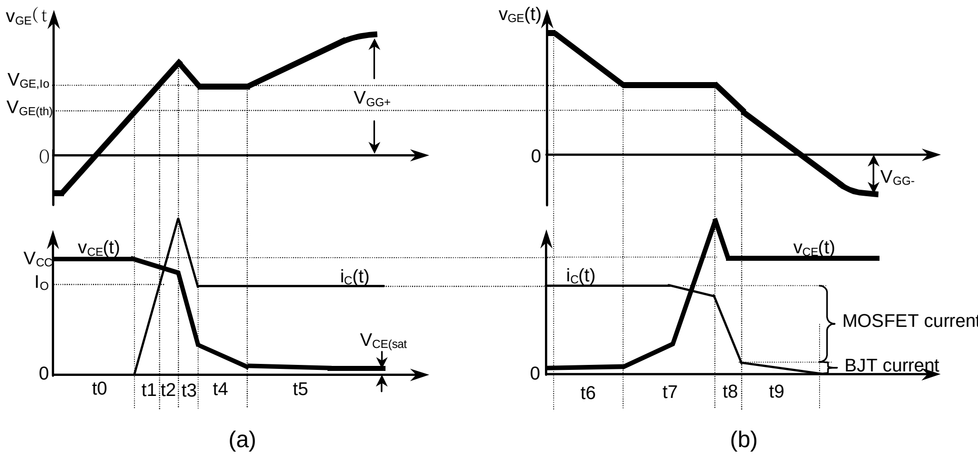


Figure 17. V_{GE}(t), V_{CE}(t), I_C(t) Switching waveforms
(a) Turn-on
(b) Turn-off

Since the input side of the IGBT has a MOS gate structure, its on and off state transition is very similar to that of a power MOSFET.

The analysis of the Turn-on transition

Turn-on switching time is determined by the charging speed of input capacitance (C_{ies}).

(1) t0 section: It is the section where v_{GE} rises to $V_{GE(th)}$ while i_G (gate current) charges the parasitic input capacitance C_{ge}, C_{gc}. The v_{GE} increase pattern is shown to be linear, but it is actually an exponential curve with time constant $R_G(C_{ge}+C_{gc})$. The v_{CE} is maintained at the V_{CC} value, and i_C remains at zero. The delay time is generally defined as the time when the gate voltage is 10% of V_{GG+} to when i_C reaches 10% of I_O value. As such, most of the turn-on delay falls under this section.

(2) t1 section: v_{GE} continues to increase exponentially past $V_{GE(th)}$ as it does in t0 section. As v_{GE} increases, i_C begins to increase to reach I_O which is the full load current. In the t_1 and t_2 section, v_{CE} appears to be shaved off than V_{CC}. This is due to the voltage induced to L_S in Fig. 16 during the increase in i_C, $V_{LS} = L_S{*}di_C/dt$. The amount it is shaved off is proportional to the magnitude of di_C/dt and L_S, and the shape is determined by i_C.

(3) t2, t3 sections: In i_D, the diode current which begins to decrease from t1 section does not immediately fall to zero, but there is a reverse recovery current where it flows in the reverse direction. This current is added to i_C current to take the same shape as i_C in the t2 and t3 section. At this time, the diode voltage recovers and increases, and v_{CE} decreases, and when v_{CE} is high, it decreases rapidly as C_{gc} takes a small value. In t3 section, C_{gc} discharges by absorbing the gate drive current and the discharged current from C_{ge}. At the end of t3 section, reverse recovery of the diode stops.

(4) t4 section: In this section, i_G continues to charge C_{gc}. v_{GE} maintains $V_{GE,Io}$ value, and i_C maintains a constant full load current (I_O). On the other hand, v_{CE} falls at a rate of $\{(V_{GG}-V_{GE,Io})/(R_GC_{gc})\}$. At this time, v_{CE} has already fallen significantly, and when v_{CE} is low, the value of C_{gc} is large. Slow charging causes a voltage tail.

(5) t5 section: In this section, v_{GE} increases exponentially to V_{GG+} with a time constant $R_G(C_{ge}+C_{gc,miller})$. At this point, $C_{gc,miller}$ is C_{gc} which increases in the low v_{CE} value due to the Miller effect. In this section, v_{CE} decreases slowly to collector-to-emitter on-state voltage and becomes fully saturated. In addition to the effect from $C_{gc,miller}$, it is because the speed of the IGBT PNP transistor portion to cross the active region to the on-state (hard saturation) is slower than that of the MOSFET portion.

(6) t6 section: This is the section that includes most of the $t_{d(off)}$ (Turn off delay time). v_{GE} falls from the injected V_{GG+} to $V_{GE,Io}$. At this time, there is no change in the values of v_{CE} or i_C.

(7) t7 section: This is the section where v_{CE} (collector voltage) increases according to the following equation, and the rate of increase can be controlled with R_G(gate resistance).

$$\frac{dv_{CE}}{dt} = \frac{V_{GE,I_O}}{C_{res} \cdot R_G}$$

(8). t_8 section: v_{CE} maintains V_{CC} value, and i_C decreases at the rate of the following equation, and its rate of increase can also be controlled with R_G.

$$\frac{di_c}{dt} = g_{fe} \cdot \frac{V_{GE,I_O}}{C_{ies} \cdot R_G}$$

As with the turn-on transient period, there is over-voltage as $V_{LS} = L_S*di_C/dt$ that is induced to stray inductance from the effect of di_C/dt is added to IGBT C-E terminals in sections t7 and 8. The MOSFET current disappears at t8, which is the first of the two sections where i_C decreases.

(9) t_9 section: PNP transistor current, out of the IGBT i_C, disappears in this section, and this current is commonly called the tail current. It takes place due to the recombination of the minority carrier (hole), which has been injected into the N- drift region during the on-state. Due to the existence of this region, the IGBT's switching characteristics are inferior as compared with a power MOSFET

SWITCHING TIME

Switching time is divided into 4 sections as shown in Fig. 18, and they are specified at T_C=25°C and 125°C for $V_{CC}=V_{CES}/2$, $I_C= I_{C,MAX}$(@T_C=100°C), V_{GE}=15V and under inductive load conditions. Data for T_C=125°C are provided to the user because the temperature of the devices in the system rise during operation. Switching time generally rises due to increases in R_G (Gate Resistance), I_C (Collector Current) and T_C (Case Temperature). Figs. 19 and 20 show detailed changes in switching time with changes in R_G, I_C and T_C. These data are not absolute values, but they are included in the data sheet as a reference for design purposes.

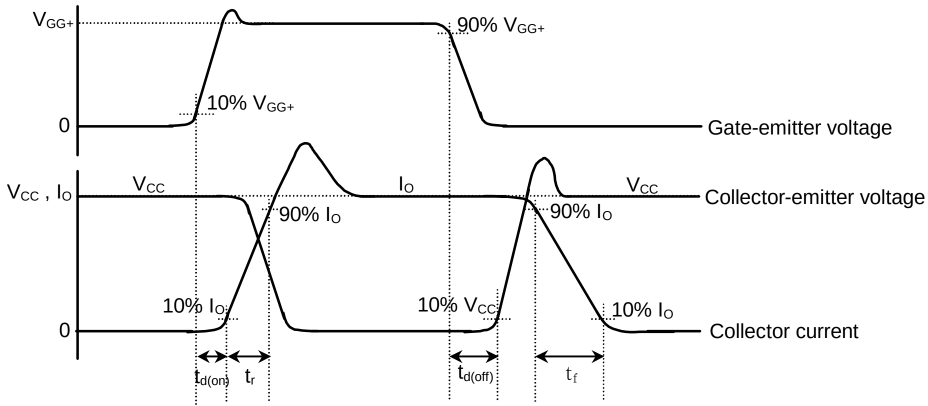


Figure 18. The Switching Waveforms of Gate-Emitter Voltage, Collector-Emitter Voltage and Collector Current

$t_{d(on)}$ (Turn-On Delay Time)

The time it takes for the collector current to reach 10% of I_O from the time a pulse is injected into the gate.

t_r (Rise Time)

The time it takes for the collector current to reach 90% of I_O from 10%. Any fall in the collector current after that point is not considered.

$t_{d(off)}$(Turn-Off Delay Time)

The time it takes for the collector-emitter voltage to reach 10% of V_{CC} from the time a pulse is removed from the gate (90% of V_{GG+}).

t_f(Fall Time)

The time it takes for the collector current to reach from 90% of I_O to 10%. We ignore the section where the collector voltage is rising and the tail current where the current is less than 10% of I_O.

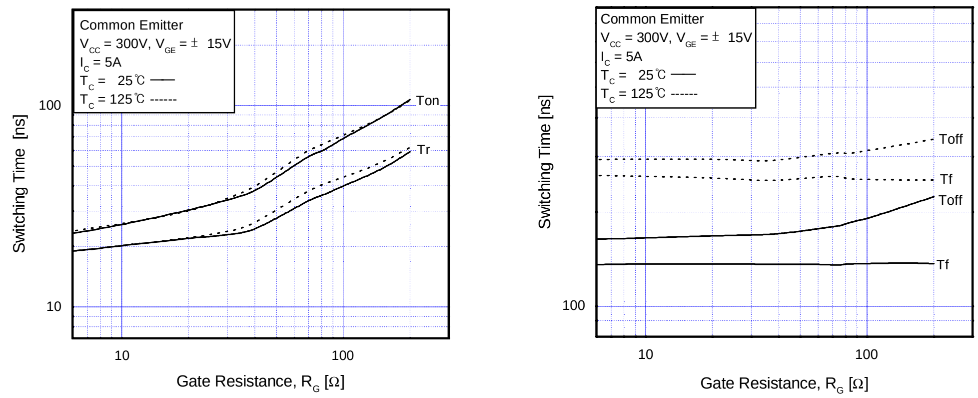


Figure 19. Turn-On / Turn-Off Characteristics vs. Gate Resistance

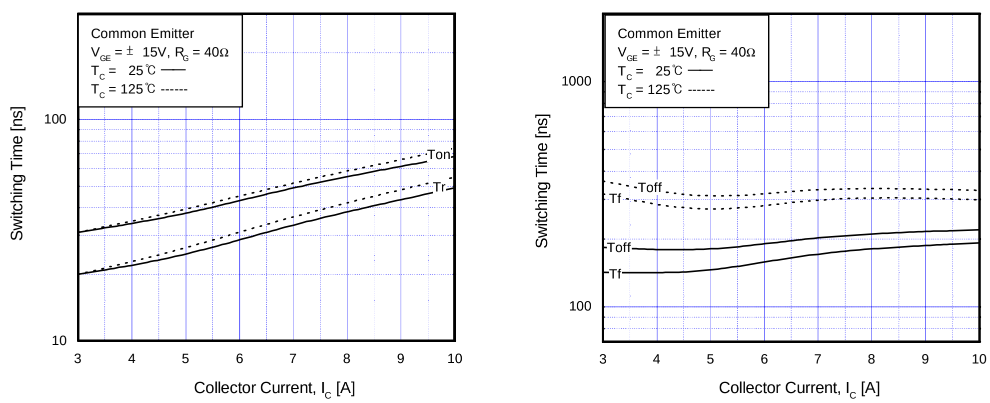


Figure 20. Turn-On / Turn-Off Characteristics vs. Collector Current

SWITCHING ENERGY

It is not enough to calculate the switching loss only with the switching time, as there is a region where some switching loss occurs although it is not specifically included in the switching time. As such, a switching energy specification is indicated for system designers in calculating switching loss. Indicating E_{off} specification would allow designers to compensate for the region where the collector-emitter voltage rises and the collector tail current that is outside the t_f region during turn-off, while E_{on} specification would compensate for the region where the collector-emitter voltage falls during turn-on. E_{on}, E_{off} and E_{ts} are specified at T_C=25°C and 125°C for V_{CC}=V_{CES}/2, I_C= $I_{C,MAX}$(@T_C=100°C), V_{GE}=15V and under inductive load conditions. Data for T_C=125°C are provided to the user because the temperature of the devices in the system rise during operation. Switching energy generally rises due to increases in R_G (Gate Resistance), I_C (Collector Current) and T_C (Case Temperature). Figs. 21 and 22 show detailed changes in switching energy with changes in R_G, I_C and T_C. These data are not absolute values, but they are included in the data sheet as a reference for design purposes.

E_{on} (Turn-On Switching Loss)

It is the amount of total energy lost during turn-on under inductive load, and it includes the loss from the diode reverse recovery. In practice, it is measured from the point where the collector current begins to flow to the point where the collector-emitter voltage completely falls to zero in order to exclude any conduction loss.

E_{off} (Turn-Off Switching Loss)

It is the amount of total energy lost during turn-off under inductive load. In practice, it is measured from the point where the collector-emitter voltage begins to rise from zero to the point where the collector current falls completely to zero.

E_{ts} (Total Switching Loss)

It only includes the energy loss in the switching region, and it is expressed as the sum of E_{on} and E_{off}.

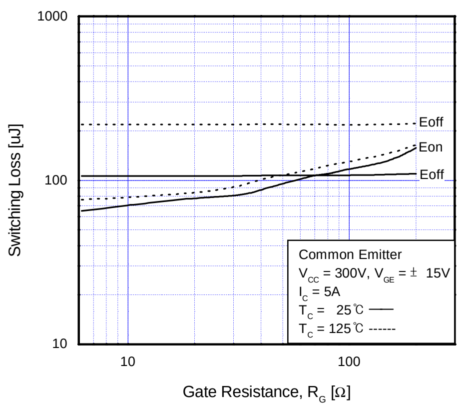


Figure 21. Switching Loss vs. Gate Resistance

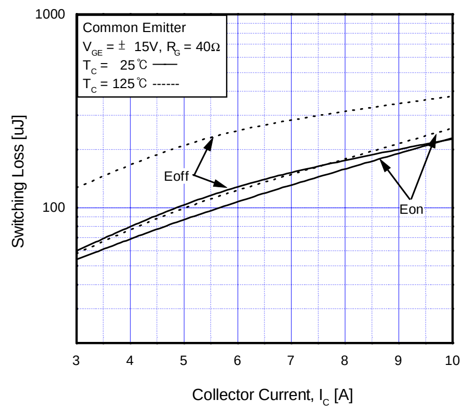


Figure 22. Switching Loss vs. Collector Current

T_{SC} (Short Circuit Withstand Time)

Fig. 23 shows an IGBT's short circuit modes in a motor drive circuit such as an error in the gate drive signal (1), shorting at the collector terminal (2), shorting at grounding (3). When it is short circuited, current, which is several times the rated I_C, flows due to the introduction of the gate bias under a large voltage between the collector and the emitter of the IGBT. If the protection circuit is not functional at this time, it would lead to the destruction of the device. It commonly takes some time (normally 3~7[µs]) for the protection circuit to become active after the over current is detected in an ordinary system. Hence, the device must be designed to withstand at least this period of time with a little margin for safety. The RUF-series, which is a short circuit rated IGBT (IGBT for use in a motor drive), is protected for a minimum of 10 [µs] under $V_{CC}=V_{CES}/2$, V_{GE}=15V at T_C=100°C conditions.

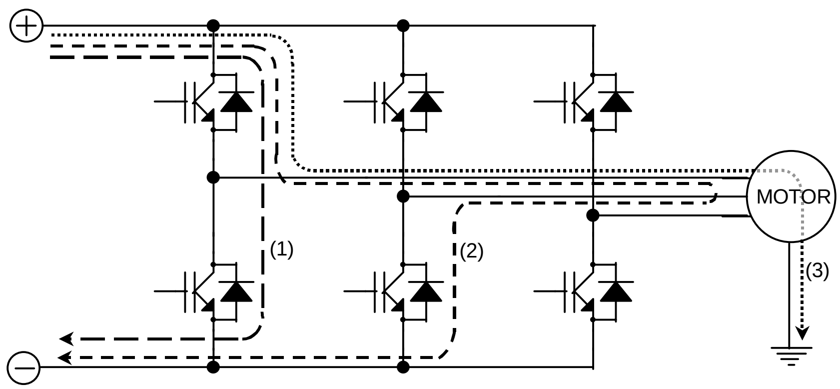


Figure 23. Short Circuit Mode of IGBT

GATE CHARGE

It is the total gate charge necessary to fully turn on the IGBT. Test criteria are set at V_{CC}= V_{CES}/2, V_{GE}=15[V], I_C= rated I_C (@T_C=100°C), which is similar to the conditions in actual operation to give useful specifications for setting the switching speed or drive circuit design. Fig. 24 shows the gate charge test circuit, and Fig. 25 shows the characteristics of the gate charge by V_{CC}. In the test circuit, a constant current source is used as the input source for the gate drive, and resistance load has been connected to make changes in I_C according to changes in V_{CC}.

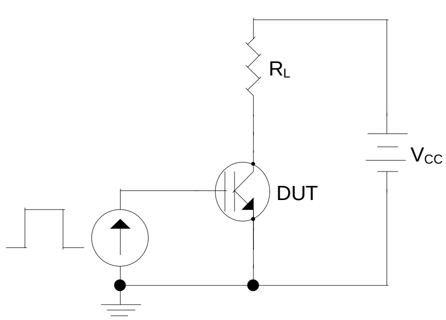


Figure 24. Gate Charge Test Circuit

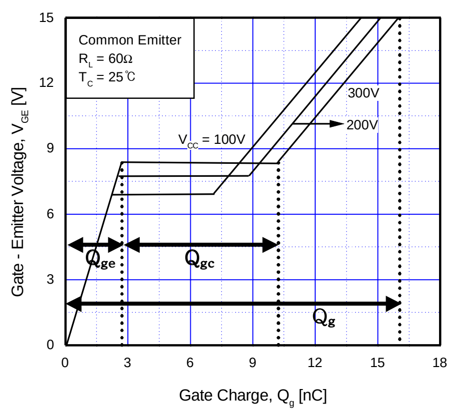


Figure 25. Gate Charge Characteristics by V_{CC}

Q_g (Total Gate Charge)

It is the total gate charge necessary to raise the gate-emitter voltage to 15V, which is necessary to fully turn on the IGBT.

Q_{ge} (Gate-Emitter Charge)

The amount of gate charge necessary to charge the gate-emitter voltage to allow specified collector current.

Q_{gc} (Gate-Collector Charge)

It is the amount of gate charge charged in the gate-collector capacitor during the flat region. In this region, the collector-emitter voltage falls from V_{CC} to on-state collector-emitter voltage, and the collector current maintains the specified collector current value.

L_e (Internal Emitter Inductance)

This is the stray inductance between the collector and emitter at a distance of 5mm from the package. The value changes depending on the length of the bonding wires between the chip and the emitter pad of the package lead frame. Typical values are 7.5[nH] for TO-220/F package, 14[nH] for TO-3P/F package and 18[nH] for TO-264 package.

4-4. Electrical Characteristics of a DIODE

V_{FM} (Diode Forward Voltage)

Diode forward voltage is specified under the maximum I_F (Diode Continuous Forward Current @T_C=100°C) and at case temperatures of 25°C and 100°C.

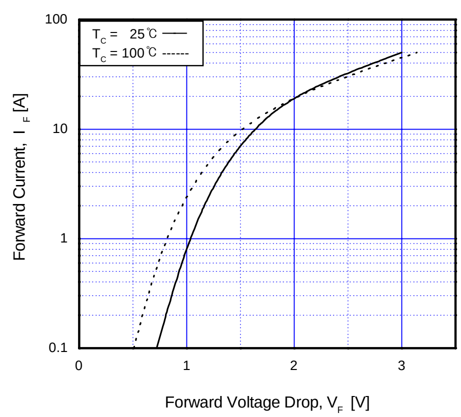


Figure 26. Forward Characteristics

T_{rr}(Diode Reverse Recovery Time) &
I_{rr}(Diode Peak Reverse Recovery Current) &
Q_{rr}(Diode Reverse Recovery Charge)

I_{rr} and T_{rr} are defined as shown in Fig. 28 in the reverse recovery region. The amount of Q_{rr}, which is charged during diode conduction and is discharged during reverse recovery region, can be calculated with I_{rr} and T_{rr} using the following equation:

$$Q_{rr} = \frac{1}{2} \times I_{rr} \times T_{rr}$$

Values of T_{rr}, I_{rr} and Q_{rr} can vary according to the test conditions, but they are generally specified at T_C=25°C and 100°C for rated I_F (Diode Continuous Forward Current @T_C=100°C) and di_F/dt = 200A/µs conditions. As shown in Fig. 27, T_{rr}, I_{rr} and Q_{rr} generally increase with a rise in case temperature. On the other hand, I_{rr} and Q_{rr} increase and T_{rr} decreases when the di_F/dt slope rises.

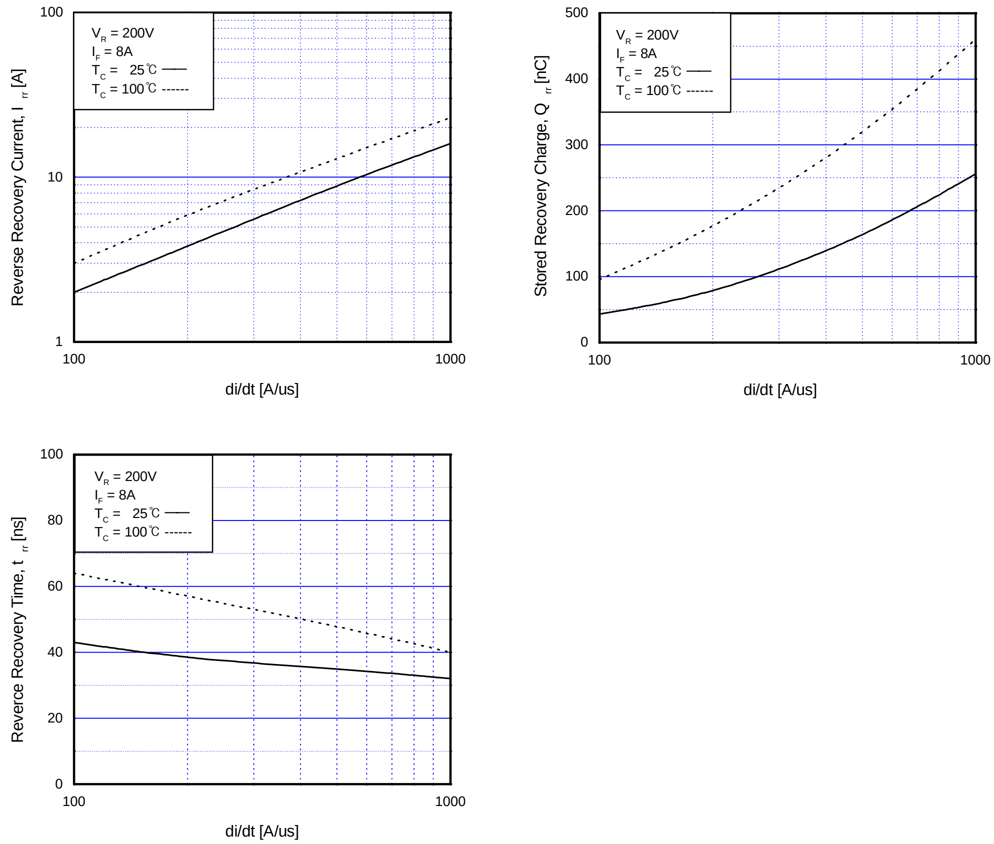


Figure 27. T_{rr}, I_{rr}, Q_{rr} Characteristics with Changes in Case Temperature, di_F/dt

Fig. 28 illustrates the test circuit and waveforms of each part for diode reverse recovery characteristics.

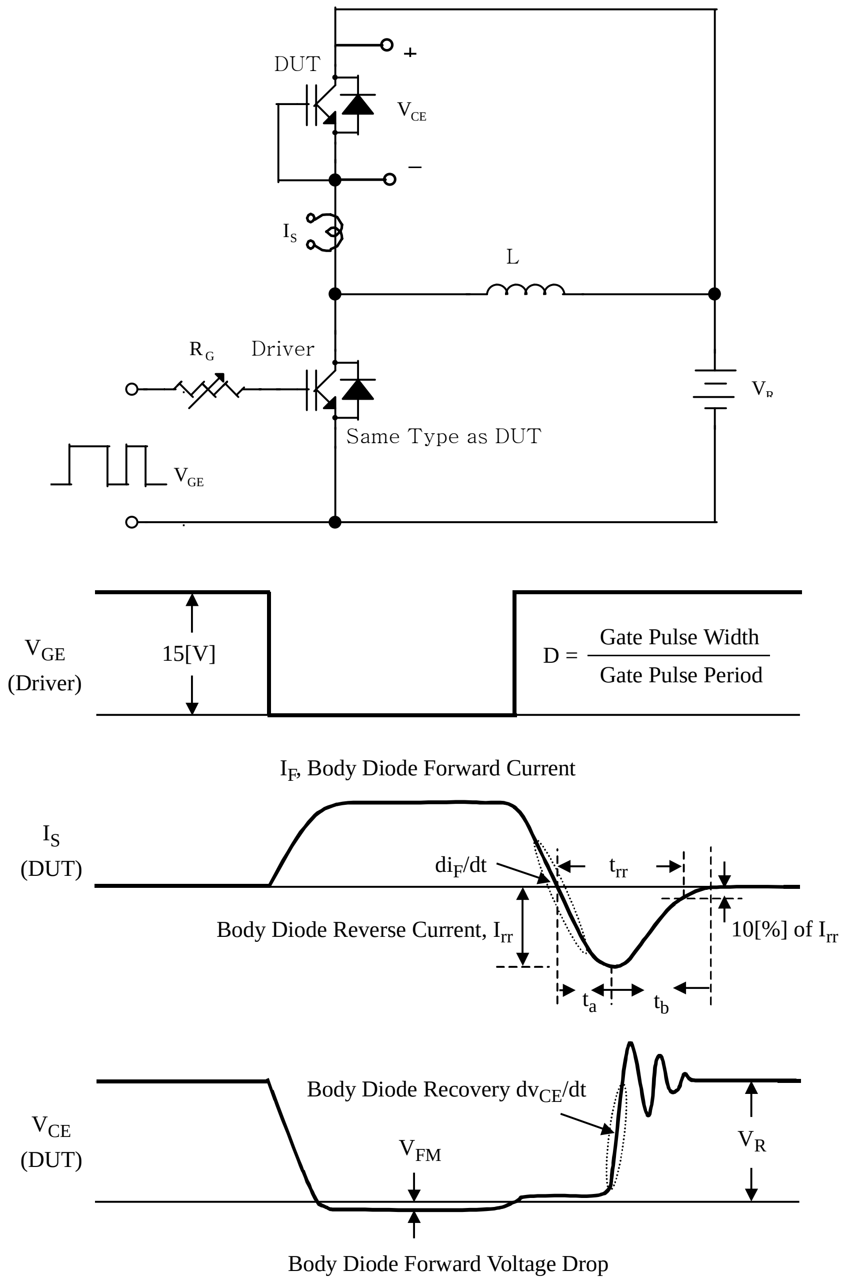


Figure 28. Diode Reverse Recovery Characteristics Test Circuit & Waveforms

TRADEMARKS

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